Design of a Fully Integrated Buck-Boost Converter ASIC

A small buck-boost converter ASIC with integrated switches on a commercial 0.35 um process node for use in a charging case for hearing devices

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Abstract

This document focuses on the pre-layout phase of a project, which was divided into pre-layout and post-layout stages. The project was initiated by Sonova AG, with the objective of designing a compact 200 mA DC/DC converter for potential integration into the charging case of their hearing devices. This first part of the documentation provides a comprehensive overview of the key steps undertaken during the pre-layout phase, including DC/DC topology selection, circuit architecture/design, and chip interface considerations. By examining these crucial aspects, this documentation offers valuable insights into the initial phase of the project, providing a solid foundation for the subsequent layout and manufacturing, and testing stages.

Acknowledgements

We are immensely grateful to our supervisor, Lars Kamm, for his invaluable feedback and guidance throughout this project. His profound expertise in the field of ASIC design has been crucial in directing us and shaping the project, enabling us to present our results here today.
We would like to express our gratitude to the faculty members of IMES (Institut für Mikroelektronik und Embedded Systems) at OST for lending us a helping hand in times of need. A special thanks goes out to Lukas Leuenberger, Simon Walker and Roman Willi for their endless hours helping us get acquainted with the tools we required and answering our many questions regarding analog circuit design.
Finally, we are profoundly grateful to Prof. Dr. Paul Zbinden for giving us this rare opportunity, to design a fully custom integrated circuit as part of our masters program.
Thank you all.

Contents

1 Assignment

1.1 Introduction

The goal of this project is to create a prototype Application Specific Integrated Circuit (ASIC) to be used inside a charging cradle for Hearing Instruments (HI) from Sonova AG. The main objective for the ASIC is to safely charge the HI from a standard USB power cable. Since there are two HI in a cradle, it must be possible to charge both HI simultaneously at their maximum charging speed. There should be a serial port to read and write data to the chip, in allow for external monitoring and configuration.

In a first step the specification shall be created and a system design proposal with ideal components should be designed and simulated. To make the chip manufacturable, these ideal components shall one by one be replaced with implementable designs from libraries or custom made, while still being able to meet the specifications. Based on the system design a layout shall be created in such a way that an ASIC can be manufactured.

Once the ASIC has been manufactured and packaged, the chip shall be validated and characterized. The measured specifications shall be compared with the requirements.

1.2 Technical Requirements

The main technical requirements of the ASIC concern the charging of the HI. The ASIC should provide a constant voltage of 5 V off of a Universal Serial Bus (USB) power supply, which can have a wide voltage range of 4.3 V to 5.3 V. As the input voltage can be higher or lower than the output, the charger must be able step up as well as step down the voltage.
Each HI can pull a maximum charging current of 80 mA, the chip therefore needs to be able to supply around 100 mA per output, in order to have some margin. Additional functionalities and safety features are allowed but not a must.

Input Voltage Range	4.3 V - 5.3 V
Output Voltage	4.9 V-5.1 V
Output Current	200 mA

Table 1: *Main requirements for the charger ASIC*

The full technical requirements can be found in the attachments.

1.3 Background of Application

The project idea originally came from Sonova AG, therefore most of the requirements were provided by them. Since the scope of the requirements is large and it's not possible to fulfil all of them in the given time and with the given resources, the focus shall be on the basic functionalities mentioned above.

1.4 | Scope of Work

1.4.1 | Project Thesis 1

- Literature study
- Specifications
- Verification
- Design for test

1.4.2 | Project Thesis 2

- Layout
- Post Layout Simulations
- Tape out
- Validation plan
- PCB for validation
- Validation
- Test report

1.5 | Goals

- Getting familiar with the various tools required for ASIC design
- Document the project and provide reasoning for important design decisions
- Understand and complete the entire ASIC design flow consisting of:
  - System design
  - Layout
  - Tape out
  - Validation
  - (optional) Redesign

1.6 | Mile stones

- Project start: 23.09.2022
- System Design: 14.07.2023
- Delivery of report 1: 14.07.2023
- Presentation one 10.07.2023
- Tape out ready: 03.11.2023
- Delivery of report 2: 21.06.2024
- Presentation two 21.06.2024

1.7 | Organization

- Advisor: Lars Kamm
- Work place: OST Rapperswil, room 8221
- Meetings: every two weeks
- Document filing: \\hsr.ch\root\auw\sge\studarbeiten\MikroelSys\MSE\MSE_-22HS_Jansky_Meyer

2 Introduction

The goal of this project is to create prototype ASIC, which can be used inside a charging cradle of a HI. Thereby the ASIC should deliver a constant voltage of 5V to reliably charge the HI from any USB supply. Which means according to the USB specification the circuit should be fully functional down to a voltage of 4.35 V. The reason of this requirement comes from the fact that the new HI's have a lithium battery inside, which require a charging voltage of up to 4.2 V. When the USB supply is then as low as 4.35 V the battery will not fully charge any more or only very slow, since the Low Drop-Out (LDO) regulator has a certain headroom and the charger also contains some contact resistances from the charger pins to the HI pins. So if one wants to charge at full speed and one assumes that the charging resistance can be several ohms this causes a significant voltage drop. [1]

The project of designing and testing such an ASIC was divided in two parts „pre-layolut phase“ and „post-layolut phase“, since the project was executed in a master program which requires two separate stages.

3 Literature Study

3.1 Intro

Since the specifications for the project were already well-defined, the primary focus of the literature research was not directed towards market analysis and existing solutions. Instead, the emphasis was placed on exploring the implementation aspects of designing an ASIC for such a specialized application.

3.2 Project Organization

For project organization, we utilized Jira. We chose this platform because one of our project participants was already familiar with it. It is a freely available tool for teams of up to ten people [2] and offers a user-friendly and transparent project management experience. Moreover, Jira enables time tracking, allowing us to analyze time allocation and make informed decisions for future projects.

3.2.1 Schedule

The schedule was given by the master program. Which means start was summer 2022 and end is summer 2024. Furthermore, the tape-in date of the ASIC manufacturer defined the date until when the ASIC design must have been completed.

3.3 Jira

Jira is an issue tracking and project management software [3] to which one finds more information on the following page.

3.4 Process Evaluation

In the process evaluation process for this project, several criteria were considered due to its affiliation with a master's program:

- The feasibility of implementing the project using a specific process.
- Familiarity of university personnel with the manufacturer and the chosen process.
- Cost-effectiveness.

Since the university has experience with processes offered by X-Fab (refer to subsection 3.6), and X-Fab provides a process that meets the project's requirements, it was determined to proceed with X-Fab. Consequently, no other manufacturers were considered during the evaluation phase. The primary technology requirement was the support for 5 V. Therefore, the decision was made to implement the project using the Multi Project Waver (MPW) approach with the «XH035 0.35 µm HV Complementary Metal–Oxide–Semiconductor (CMOS) 4M» process and the MOS and MOS5A module. Additional information about this process can be found in subsection 3.5 and **??**.

3.5 XH035 Process

The XH035 process has four main process modules, which can be combined with one or more additional modules. An overview can be found below:

- MOS (3.3 V)
- MOS5 (5 V)
- MOSLL (3.3 V low leakage)
- MOSLT (3.3 V low threshold)

For this project, the MOS5 module would be the most suitable, but since there is no MPW available one of the others must be chosen with the addition of MOS5A [4]. [1]

3.6 X-FAB

X-Fab it as pure play foundry, which means they only manufacture devices for other companies, without designing them [5], Specialized in analog/mixed-signal semiconductor technologies [6].

3.7 DC/DC Topology

There are multiple topologies of DC-to-DC converters in active use with step-up (boost) and step-down (buck) capabilities as required in this project. In this chapter we are going to introduce various topologies, their advantages and disadvantages in order to find a suitable fit for our requirements. Our main criteria are as follows:

- Few external components
- Few connections to external components
- Non inverting

The selected topology will be implemented on a single ASIC, therefore we have additional requirements as opposed to a discrete implementation. Large capacitors and inductors

[1] All the information mentioned can also be found in the datasheet [4]

can't be integrated into the chip and have to be external to the design. External components obviously need to connected to the chip and require pads, which adds size and complicates routing. This leads to a strong incentive to keep the number external components to a minimum and is our main concern. The other listed requirements are of lower priority.

3.7.1 | SEPIC

A Single-Ended Primary-Inductor Converter (SEPIC) is type of switching converter which is able to operate from an input voltage lesser, greater or equal to the output voltage as need in this application. It requires only one active component, Q1 as it can be seen in Figure 1 [7]. It however requires two external inductors, an external coupling capacitor and an output smoothing capacitor. The SEPIC topology has widespread adoption and has been extensively researched and documented. Its high efficiency [8] and lower stress on components compared to Cuk and buck-boost converters [9] are large advantages, however this topology is not well suited for high levels of integration as needed in this application. The number of external components is quite high with two inductors, two capacitors and depending the implementation one diode. The diode could be integrated into the ASIC, this however makes little sense, since both electrical connections are exclusively connected to external components.

Switching Elements	1
Ext. Inductors	2
Ext. Capacitors	2
Ext. Diodes	1*

Table 2: *Elements of a SEPIC converter*

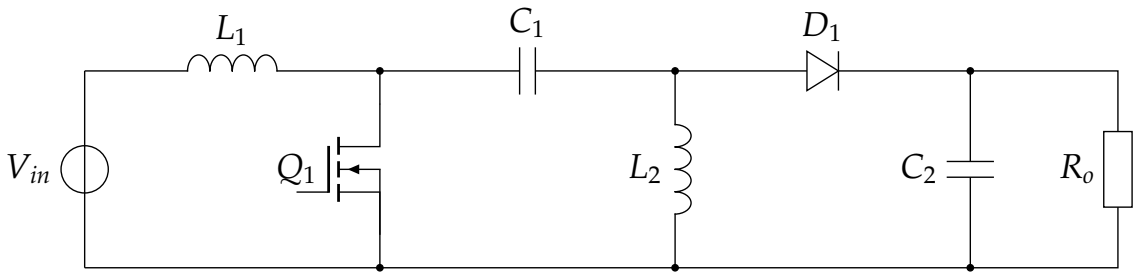


Figure 1: *Example of a SEPIC converter*

3.7.2 | Cuk

The Cuk converter is another type of buck-boost converter, which has the main advantage of reducing the ripple current on the input and output. It therefore has near continuous input and output currents which is its main advantage in comparison with the other converter topologies introduced in this chapter. The number and types of components are identical to the SEPIC design and only differs in their wiring. Thus it suffers from the same drawback of being difficult to integrate into a single chip.

Switching Elements	1
Ext. Inductors	2
Ext. Capacitors	2
Ext. Diodes	1*

Table 3: *Elements of Cuk*

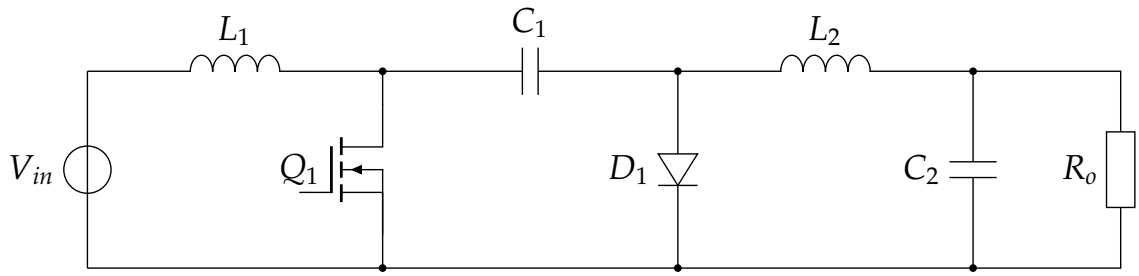


Figure 2: *Example of a Cuk converter*

3.7.3 | Cascaded Boost-Buck Converter

Using the basic building blocks of simple buck and boost converters, it is possible to cascade the two in order to create a Boost-Buck-Cascaded or a Buck-Boost-Cascaded converter. The Boost-Buck-Cascaded topology uses a basic boost converter followed by a basic buck converter. This design requires a minimum 2 switching transistors and uses 2 external inductors. This design requires a large capacitor after the first stage, which would have to external to meet the capacitance required.

Switching Elements	2
Ext. Inductors	2
Ext. Capacitors	2

Table 4: *Elements of Boost-Buck-Cascaded*

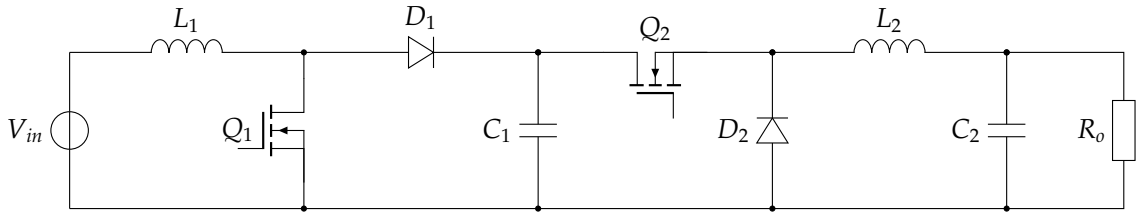


Figure 3: *Example of a cascaded boost-buck converter*

3.7.4 | Cascaded Buck-Boost Converter

Switching the order of the simple buck and boost converters we get the Buck-Boost-Cascaded topology. In this configuration one single inductor is shared for both the up- and down-conversion. Additionally the only capacitor required is an output smoothing capacitor, as is the case with all other topologies. This configuration also lends itself for the use of synchronous rectification to further improve efficiency.

Switching Elements	2
Ext. Inductors	1
Ext. Capacitors	1

Table 5: *Elements of a cascaded buck-boost-converter*

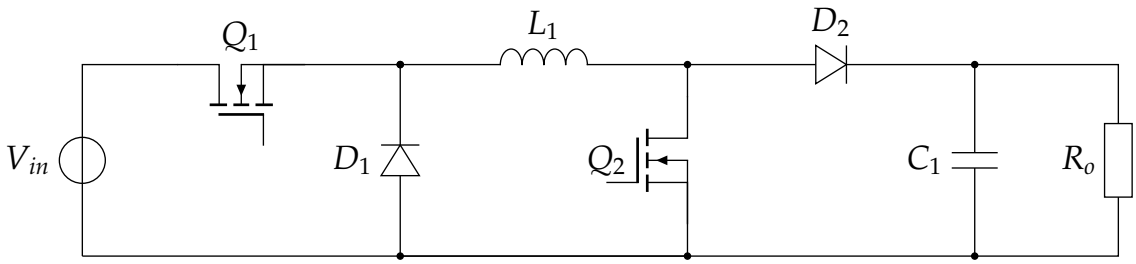


Figure 4: *Example of a cascaded buck-boost converter*

3.8 | Controller structure

The main objective of the DC/DC converter is to create a stable output voltage, regardless of the input voltage and load present on the output. It therefore may seem appealing to only use the output voltage of as a regulation variable. Such a scheme would have no regard for the current flowing in the inductor, which leads to bad regulation characteristics and could have catastrophic consequences, if the current exceeds the current ratings of the used components. Therefore many commercial converter designs additionally measure the current flowing in the inductor and use regulation loop to control it. This control loop can be quite rudimentary for instance only ensuring, the current doesn't exceed a certain value or they can be elaborate by regulating the output current with a sophisticated regulator design. The former control scheme is referred to as peak current-mode control, while the latter is called average current-mode control. Both approaches are in commercial use today.

3.8.1 | General Current-Mode Control

The basic idea of current-mode control is to have two superimposed controllers, one for the inductor current and one for the output voltage. The faster inner control loop regulates the inductor current to a value set by the outer voltage control loop. The slower outer control loop aims to regulate the output voltage. Using these superimposed control loops allows both to be tuned independently in order to improve the regulator performance. This method actively regulates the current in the inductor and by extension the switching devices, making it possible effectively limit and control the inductor current.
As an example, if the inner loop is in steady-state, but the output voltage is to low, the outer loop increases the set current of the inner loop. The increased inductor current thus leads to more energy being transferred in to the output capacitor, increasing the output voltage. The main difference between the peak and average current-mode control is in how the inner current control loop is implemented. Both operate with the same two loop operating principle.

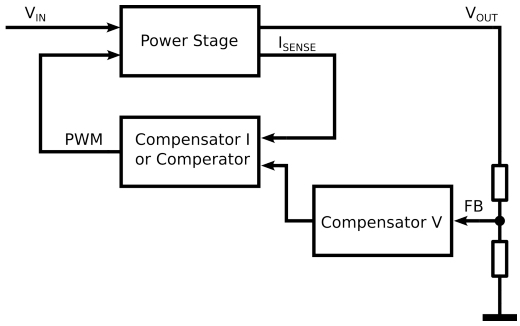


Figure 5: *Schematic prepresentaion of current-mode control*

3.8.2 | Peak Current-Mode Control

The older of the two approaches is peak current-mode control first described by T. A. Froeschle in 1967 and Cecil of Bell Labs/Western Electric in 1978 [10] in order to prevent transformer cores from saturating. In this type of current-mode control, the inductor current is allowed to increase until a threshold is reached. This is usually done by using a comparator to compare the current through the inductor and a threshold given by the outer loop. The output of the comparator is then used to reset the latch driving generating the drive signals for the power stage. This control scheme is still in use and is available in most integrated buck-boost converters such as the LM5175 from Texas Instruments[11]. Peak current-mode control is well understood and has the advantage of only requiring the measurement of the inductor current when it is rising. It also implicitly acts a current limiting circuit, since as soon as the current exceeds the predetermined value, the transistor charging the inductor switches off, thus limiting the current flow through the inductor. This scheme is also more suitable for low inductor currents. This is due to the peak current level being significantly higher than the average current level, thus having greater signal levels. The peak current-code control and its analog the valley current-mode control are however inherently susceptible to noise on the feedback line, since noise spikes can cause the comparator to switch prematurely thus resetting the latch[10]. There are ways around this problem, for instance using emulated current-mode control, this however further increases design complexity. For duty-cycles greater than 50 % peak current-mode control also requires an additional slope compensation circuit to eliminate subharmonic oscillations[10][12].

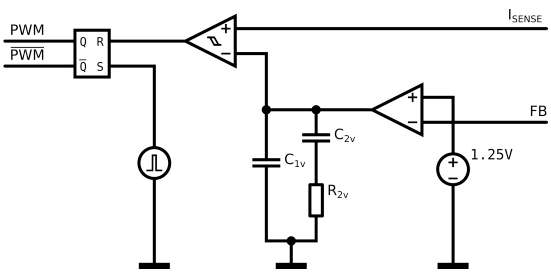


Figure 6: *Structure of the control loop for peak current-mode control*

3.8.3 | Average Current-Mode Control

The more modern approach is to use a filter network to approximate the average current flowing in the inductor and regulate the inductor current based on this value. This technique has multiple advantages. By filtering the inductor current signal, the regulator becomes less susceptible to noise on the feedback line. It also removes the need for slope compensation at high duty-cycles and allows the use of a high gain amplifier in the current feedback loop[10]. Average current-mode control however requires the sensing of the entire inductor current waveform. This eliminates the possibility of using the $R_{DS,on}$ of a single switching transistor as a current shunt.

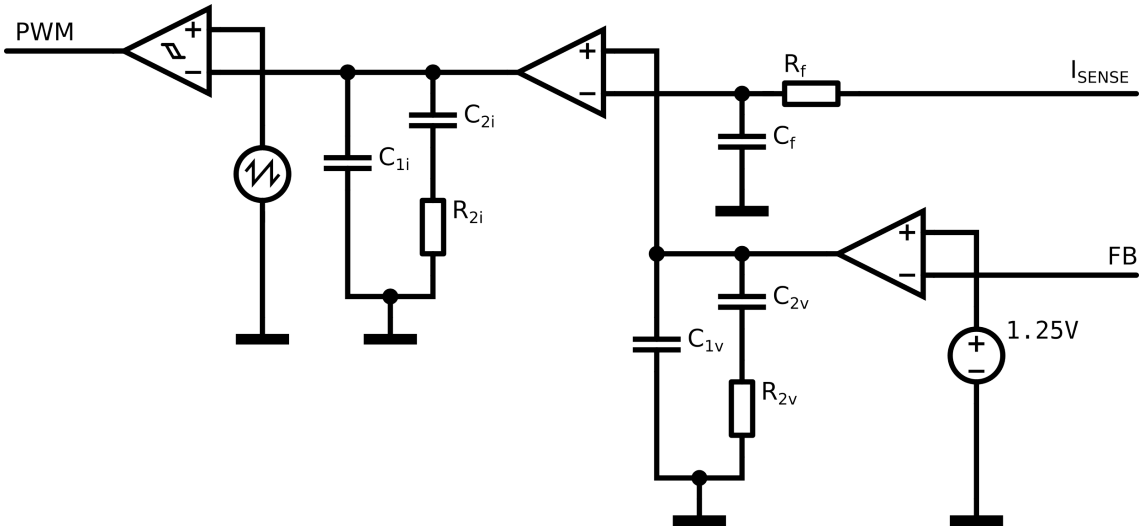


Figure 7: *Structure of the control loop for average current-mode control*

3.9 | Slope Compensation and Sub-Harmonic Oscillations

Switching Converters based on a fixed frequency peak current-mode control are susceptible to phenomenon called sub-harmonic oscillations when operating at a duty-cycle greater then 50 Other control modes are also effected from this phenomenon with varying conditions in which it takes place, in this chapter we will only be evaluating its effects on peak current-mode control. Sub-harmonic oscillations is the name given to this phenomenon of oscillations in the inductor current when operating in a steady state as can be seen in figure Figure 8B. These oscillations occur in a lower frequency than the switching frequency of the converter and are caused by the inductor current not returning to the start value at the end of the switching cycle. The inductor current should have triangular waveform, oscillating from some minimum value to some maximum value and back in one switching period. As can be seen in figure Figure 8B, this is not the case when sub-harmonic oscillations are present. Sub-harmonic oscillations are generally not harmful[13], but they can cause audible noise if the oscillations lie in the audible frequency spectrum.

To guarantee a sub-harmonic oscillation free operation using peak current-mode control at high duty-cycles, a technique called slope compensation is employed. Slope compensation reduces the peak current threshold proportional to the pulse width of the ongoing

switching cycle. When correctly implemented, this ensures the inductor current always returns to the value at the start of the switching cycle, eliminating sub-harmonic oscillations in the process. The formulas to calculate the ideal magnitude of slope compensation required are well documented and can be found for most switching converter topologies. Slope compensation eliminating sub-harmonic oscillations can be seen in Figure 8C.

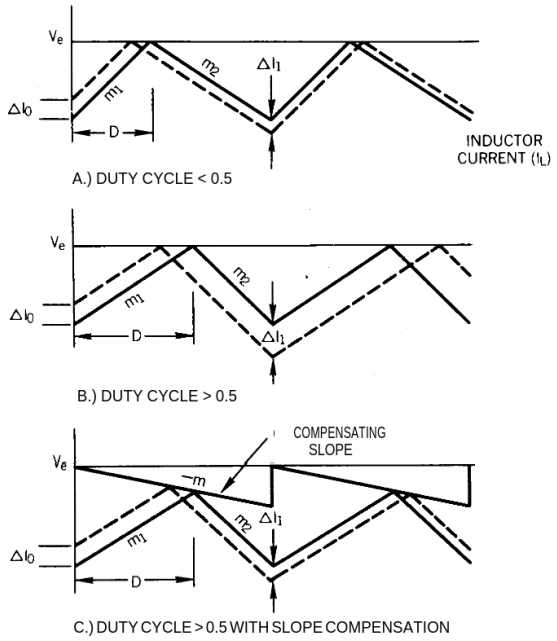


Figure 8: *Subharmonic oscillations in peak current-mode control with $D > 0.5$ and how slope compensation can eliminate them[14]*

3.10 | Synchronous Rectification

The diodes in switching converter designs are often replaced with active switches in practice called active or synchronous rectification. This is done to improve efficiency by reducing the power dissipation of the circuit. The diodes in switching converters are used to allow current flow in one direction, but not the other. These diodes are suitable for the this task, have the drawback of producing a forward voltage drop of around 0.6 V when conducting current. In scenarios in which currents are sufficiently high and the converter requires high efficiencies, the power dissipation created in the diodes becomes non negligible. To reduce the power dissipation of the circuit, the diodes are often replaced with MOSFETs as an active switch. By turning on the MOSFET during the time when the diode would be conducting and turning it off when the diode would be blocking the function of the diode can be replicated. The power dissipation from this practice is often less than the power dissipation from a diode, as the inequality Equation 1 holds for most realistic applications. In practice, this drive pattern is simple to implement and can greatly improve the overall efficiency, which explains its the widespread use. All buck-boost converters with integrated switches examined as part of this project employ synchronous rectification.

$$P_{diss,MOSFET} \approx R_{DS,on} * I_L^2 < P_{diss,diode} \approx V_F * I_L \tag{1}$$

3.11 Modulation Schemes in Switch-Mode Power Supplies

There are multiple different modulation schemes in use in switch-mode power supplies, each with a different advantages and disadvantages. The simplest scheme is pulse width modulation, where the amount of energy transferred from the input to the output is modulated with the width of the pulse. Pulse-Width Modulation (PWM) schemes switch in a fixed frequency and change the on time depending on how much power is supposed to be transferred. A simple pulse-width modulation can be achieved by comparing to be modulated signal with a sawtooth waveform. Such PWM based control schemes are found in simple converter designs and in more complex converters, when sufficient load is present. These more complex converters often use pulse frequency modulation under light loads. In Pulse-Frequency Modulation (PFM) the pulse width is fixed width and instead the frequency or the time in between pulses is varied. Controllers such as the TPS63900 employ completely different modulation schemes.
Converters such as the cascaded buck-boost converter in 9, can generally be used in three modes of operation, depending on how the two transistors are driven. It is possible to use the circuit in buck, boost and buck-boost mode. If both switches are modulated on and off it is possible to boost the output voltage as well es buck it. By only driving one of the switches, the circuit turns in to the conventional boost-topology or buck-topology, depending on which switch is is actively driven. The static switch obviously needs be in the correct state for the required mode of operation. Only driving one transistor reduces switching losses, at the cost of only being able to do one type of conversion.

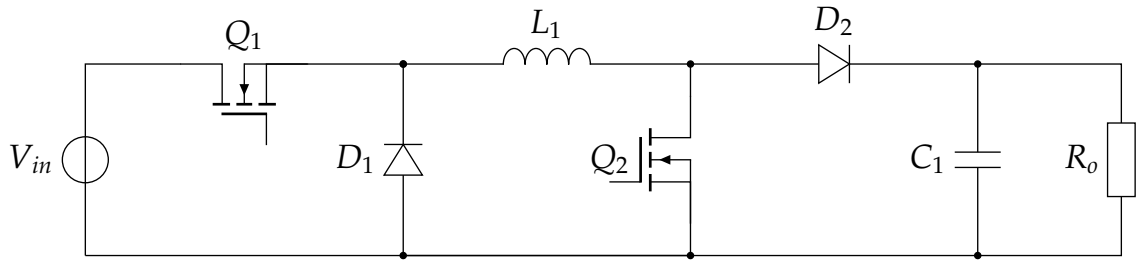


Figure 9: *Circuit of two switch cascaded buck-boost converter*

3.12 Multi Mode Controllers

A common sight in modern buck-boost converters are controllers with multiple operating modes. The use of multiple operating modes is done to improve efficiency and improve regulation characteristics in different scenarios. A common occurrence is the use of PWM based operating modes for normal operation and PFM operation for light loads. As it can be challenging to accurately sense currents around 0 A, it is easier to change to PFM and rely entirely on voltage feedback. PFM is also employed due to its higher efficiency, as is requires fewer switching cycles when operating with small loads compared to PWM. Another approach is used in converters with very wide operating ranges. They include up to three different modes, one for pure buck conversions, one for buck-boost

operating mode for when the input and output voltages are similar and one for pure boost conversions[15]. More common are controller with only a buck converting mode and a buck-boost converting mode as boost operation is seldomly used and the slight efficiency penalty is a worthwhile trade of for the simpler design[15]. A multi mode controller greatly increases design complexity as it not only requires the implementation of multiple different control schemes, but requires a smooth transitions between them.[15] In design with narrow operating ranges, the number of operating modes are often reduced to simplify the design. The Integrated Circuit (IC) designer as Texas Instruments recognized this problem and found an interesting solution. ICs such as the TPS63900 use their own modulation scheme, which is more complicated than the modulation schemes presented here, but this scheme allows them to achieve high efficiency over the whole input and output range. In this way, they do not have to implement multiple operating modes and ensure safe transition between them, but were able to created one complex operating for the whole operating range.

3.13 Blanking Time

The process of switching the large switching devices in switching power supplies can cause a lot of noise, especially on nodes with high impedances [16]. In the case of peak current-mode control, this noise could cause the controller to register the current exceeding the peak prematurely[16]. Additionally various capacitances on the large switching devices need to charged or discharged, causing large currents flow for short periods after the switching event. It also possible, that the current measurement needs some amount of time to start tracking the current accurately. Do to these reasons it is often beneficial to implement a blanking time in controllers using peak current-mode control. The blanking time is the name given to a brief time, in which the circuit disregards some or all of its inputs. For peak current-mode control a RS latch creates PWM drive signals for the switching devices. The latch is set from a timer in a fixed interval and reset once the current limit is reached. In this case, a blanking time is used in between the time the latch was set and the earliest time it is allowed to be reset. This guarantees a minimum duty-cycle and inhibits premature resetting of the latch. The amount of blanking time needed is implementation dependent, but is typically in the order of tens to hundreds of nano seconds.

3.14 Current Sensing

An essential part of any control approach using current-mode control is the ability to accurately measure current. In switch mode power supplies in particular, it is important to accurately measure the current flowing in the inductor. The list methods presented here are by no means exhaustive, but represent the methods considered for this project. The probably most straight-forward means to measure the current flowing in the inductor, is to add a shunt resistor in series to the inductor and measure the voltage drop over it. While on the surface this method may seems very simple, it brings a lot of hidden technical challenges. First of all, the shunt resistor constantly dissipates power, lowering efficiency. Additionally it is difficult to embed the sense resistor on the chip, due to

difficulties to design it into the layout. It would also require the operational amplifier amplifying the voltage drop to have very high common mode rejection ratio. This is due to the node voltage switching from around 0 V to 5 V and back during each switching cycle. The error introduced would have to be small enough to not negatively effect the current measurement, even when measuring low currents.
The second method considered is the SenseFET technique, which measures the current in the large switching Field-Effect Transistor (FET)s by mirroring the current flowing through them. The current in the large transistor mirrored with some large scaling factor into the SenseFET, from where it can be easily be further mirrored or turned into a voltage. For the SenseFET to operate in a mirroring manner, additional circuitry is obviously required. This method is well explored and there are many papers with example implementations available. This technique introduces to no additional external components or power dissipating resistors into the design, which are very desirable characteristics.

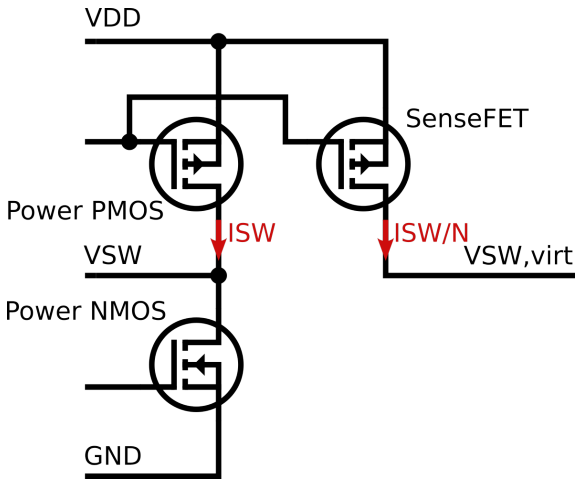


Figure 10: *Schematic representation of a SenseFET based current measurement*

Another method is to use the on resistance of the switching device $R_{DS,on}$ as a shunt resistor. The on resistance of the transistor can be obtained by running simulations and is therefore a known quantity. It is therefore sufficient to amplify the voltage drop over the transistor and measure that, to obtain information on the current flowing through the device. The on resistance is unfortunately temperature dependent and can change over the process corners. While this is not ideal, it is far less complex to implement compared with the SenseFET method. If required, it can implemented in a way, which also allows the measurement of bidirectional current flow. As this method utilizes an intrinsic property of the switch, no additional components and heat dissipating devices are introduced.

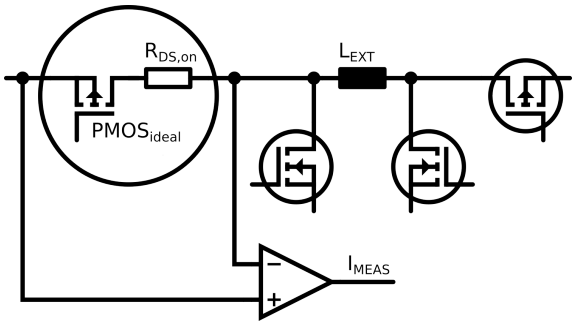


Figure 11: *Schematic representation of a $R_{DS,on}$ based current measurement*

3.15 | Over-Current Protection

Current limiting or over-current protection is the practice of limiting the current that may be delivered to a load in order to protect the load and the source. In power supplies the is often achieved by measuring the output current or an other value proportional to it and modifying the converters behavior if an overload condition is recognized. Based on the type of controller different, different ways are used to recognize over load conditions. Average current-mode controller generally recognize an overload condition based on the average current in the inductor and peak current-mode controller recognize over current based on the peak current flowing in the inductor. In some high power peak current-mode controllers, an additional average current measurement is used to allow for constant current behavior[11].

A current limit can behave in a variety of different ways. The simplest, is to have a hard current limit that can not be exceeded. The source behaves as a constant voltage source until the current rises above the threshold, after which the source switches to a constant current operation, delivering the maximum current allowed. Increasing the load any further only reduces the output voltage, the current stays the same. Even with a complete short circuit on the output, only the set maximum current is allowed to flow.

When the maximum output current is further decreased with increasing load, this called foldback behavior. Reducing the output current with increasing loads allows for a reduction in component stresses during an overload condition compared with the hard current limit. In the extreme case of a short circuit on the output, the current can be limited to small proportion of the current in normal operation.

While the previous two approaches are useable for switching as well as linear supplies, the hiccup current limitation technique is only applicable to switching supplies. In the previous two approaches, current was still supplied to the output during in overload conditions, even though the overload condition is in many cases only present when an error occurred. As such, it makes sense to recognize this as an error condition and stop the power going to the load. During hiccup operation, the converter tries to supply power to the load and if the converter detects an overload condition it stops the switching[17]. After waiting some time and it tries to start back up. Many specifics are implementation dependent, but often a counter is used to count the number of switching cycles, where an over-current event was detected. After reaching the limit, the switching operation is

halted for some time, before it tries to supply power to the load again[17]. The limit is often user selectable. If the large load is removed, the converter starts back up in normal operation, otherwise it counts back up to the maximum number of over current events allowed before turning back off, leading to a behavior that resembles hiccups.

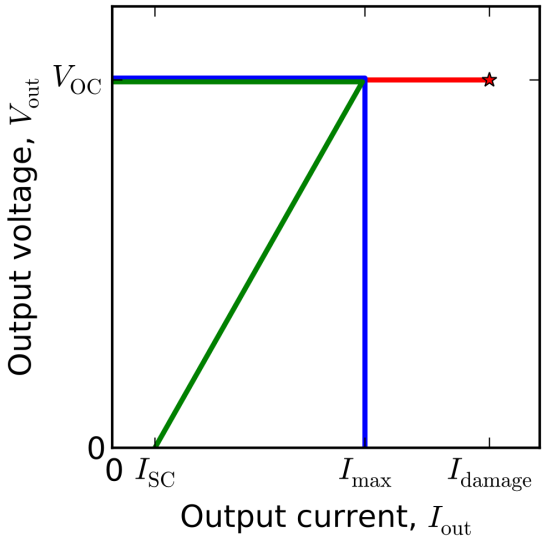


Figure 12: *Overload handling behaviors: foldback, constant current, unlimited*

3.16 Soft-Start

A common feature of modern switching controllers is a so called soft-start behavior, which aims to limit inrush currents by slowly ramping up the output current after the converter is turned on. The two main implementations are either time or output voltage based. In time based implementations, the output current is ramped up for a set time interval, after it reaches its nominal value. This approach is more common in high power designs and makes it simple to have user configurable time, which can be set with an external capacitor. The other approach is to dynamically limit the current based on the current output voltage of the converter and can be found in smaller more integrated converter designs. Limiting the output current based on the output voltage can have the additional benefit of creating a foldback current limiting characteristic. This foldback characteristic limits the output current more, the higher the overload condition, as described in subsection 3.15. Both approaches are in widespread use and can found in a plethora of converts on the market.

3.17 Hardware Communication Protocol

To enable the transmission of status information to an external microcontroller or facilitate specific configurations of the DC/DC converter, it was decided to incorporate a communication protocol. The evaluation process aimed to identify the most suitable protocol for the project, considering the following requirements:

- Compatibility with a wide range of microcontrollers available on the market.
- Ease of implementation.

Three interfaces, namely Universal Asynchronous Receiver/Transmitter (UART), Inter-

SPI mode	Clock polarity (CPOL/CKP)	Clock phase (CPHA)	Clock edge (CKE/NCPHA)
0	0	0	1
1	0	1	0
2	1	0	1
3	1	1	0

Table 6: *SPI modes [18]*

Integrated Circuit (I2C), and Serial Peripheral Interface (SPI), fulfilled these requirements. However, after careful consideration, SPI was chosen as the preferred option. It proved to be the easiest to implement while still meeting all necessary criteria. Additionally, SPI offers the following advantages:

- Synchronous
- Addressing is very easy ⇒ read the status of a pin
- Receiving and sending data ⇒ like a shift register

By selecting SPI, the project achieves a reliable and efficient hardware communication protocol that satisfies its requirements.

3.17.1 | SPI

SPI stands for Serial Peripheral Interface. The interface consists of four logic signals:

- SCLK, SCK, CLK or SCL: Serial Clock (output from master)
- MOSI: Master Out Slave In (data output from master)
- MISO: Master In Slave Out (data output from slave)
- CS /SS: Chip/Slave Select (often active low, output from master to indicate that data is being sent)

Furthermore it can be operated in four different modes, which depend on the clock phase and the clock polarity as it can be seen in Table 6 and Figure 14 [18]. In this project it was decided to go with SPI mode zero, to which one can find an example sequence in Figure 13.

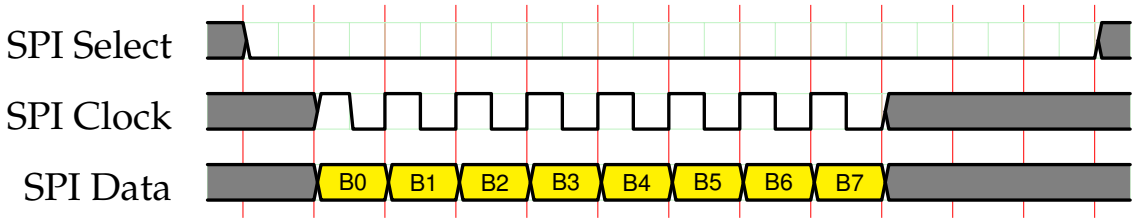


Figure 13: *SPI mode zero overview [19]*

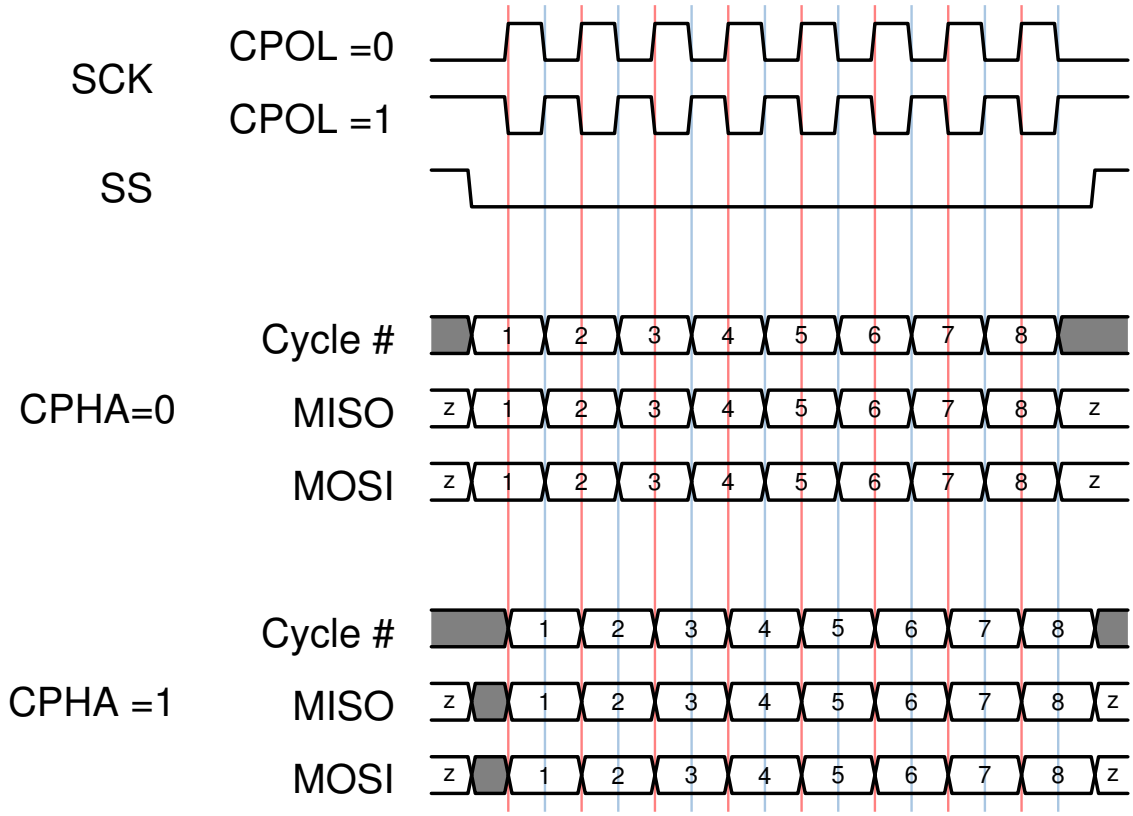


Figure 14: *SPI modes overview [19]*

3.18 Auxiliary Blocks

In addition to the main functionality provided by the DC/DC converter, a comprehensive analysis was conducted to identify the necessary auxiliary blocks required for a fully functional chip. Several essential blocks were identified, including:

- Reference Current: To feed the amplifiers utilized in the DC/DC converter and other blocks with a constant current.
- Reference Voltage: A consistent reference voltage is required to maintain an accurate DC voltage on the output.
- POR Circuit: A POR circuit is vital to ensure the system starts in a well-defined state. It generates the enable signal that initializes the chip upon power-up, guaranteeing a reliable and predictable starting condition.
- Clock Generation: Both the DC/DC converter and the digital part of the chip require a clock/sawtooth.
- Electrostatic Discharge (ESD) protection: To protect the circuit from voltage spikes.

Considering the limited time available for the project, it was decided to thoroughly investigate the implementation options for each of these auxiliary blocks. By examining and addressing the design considerations and methodologies specific to each element, the aim was to integrate them seamlessly into the overall chip design, enabling a functional and efficient system.

3.18.1 | Bandgap Reference

In the literature review, an analysis was conducted to determine if a bandgap reference was already available in the design kit provided by X-Fab. It was discovered that a bandgap reference was indeed available; however, it was designed for the 3.3 V process, while the project required a 5 V reference. Despite this discrepancy, it was decided to utilize the bandgap design and architecture from X-Fab as a starting point, with the intention of modifying and replacing the existing 3.3 V components with suitable 5 V parts.

Consequently, no further literature research was conducted specifically on bandgap designs. However, it is important to acknowledge that a thorough understanding of the bandgap concept is necessary in order to successfully adapt the design from 3.3 V to 5 V. Simply replacing the 3.3 V transistors with 5 V transistors is not a sufficient solution.

3.18.2 | Reference Current, POR Circuit, Clock generator

As the Bandgap Reference also those blocks are very often used in an ASIC. Therefore no special literature research was conducted on those components too. Instead it was analyzed what kind of standard circuits are available. Thereby it turned out that it is not possible to adapt a circuit from X-Fab, therefore another source was required. For the clock it was decided to go straight forward and to generate it with a sawtooth generator. The POR and reference current circuits were adapted from designs provided by Lars Kamm.

3.18.3 | ESD protection

In this project ESD requirements were not specified, as we do not have the required infrastructure to test ESD susceptibility adequately. Nevertheless ESD an important topic and ESD protection should be investigated when possible. Therefore a special literature research was done on this topic.

Since large P-type Metal-Oxide Semiconductor (PMOS) transistor were used inside the DC/DC converter of the charger some ESD functions could possibly be implemented in those switches of the charger. To clarify the possibility the topics latchup and snap back were investigated [20].

3.18.3.1 | Snapback

The Snapback effect is related to the Bipolar Junction Transistor (BJT) and is a mechanism where an avalanche breakdown or impact ionization provides a base current to turn on the transistor. When one speaks from Snapback it is mostly an effect that is wanted, for example for ESD protection. Instead of the Snapback effect one could use a ESD protection device with a turn on characteristic, like a Zener diode. A comparison between the two protection methods can be found in Figure 15. Where one finds on the left the I-V characteristic of an turn on ESD protection and on the right the I-V characteristic of an ESD protection based on the Snapback effect [21].

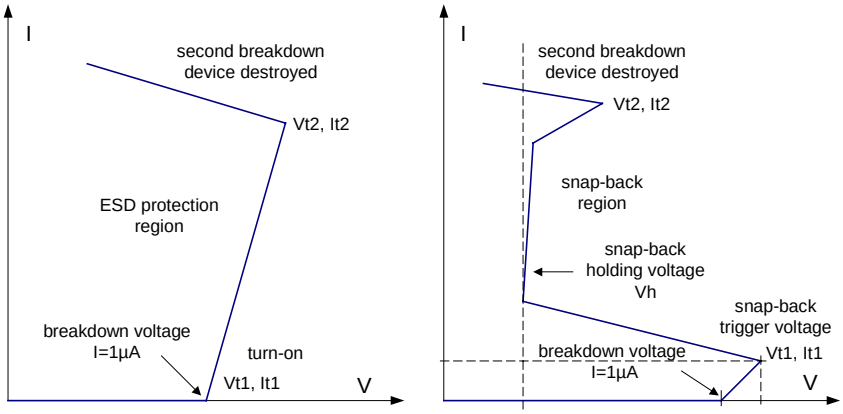


Figure 15: *Typical turn-on and snap-back characteristics of ESD protection structures ([20] p.22)*

Functional Description of the Snapback effect A high voltage occurs at the I/O pad in Figure 17. This voltage is higher than the reverse breakdown voltage of the diode that is formed between the substrate/bulk and the drain. Since the p-well has some resistance the base of the NPN BJT has a higher voltage than the emitter ⇒ the NPN BJT starts to conduct and therefore reduces the resistance from the drain/emitter to the source/collector. ⇒ The voltage on the I/O pad drops from I_{t1} to I_H even if the current on the pad increases. After that one is in the snap-back region and the current can be increased until the second breakdown voltage where the transistor gets finally destroyed.

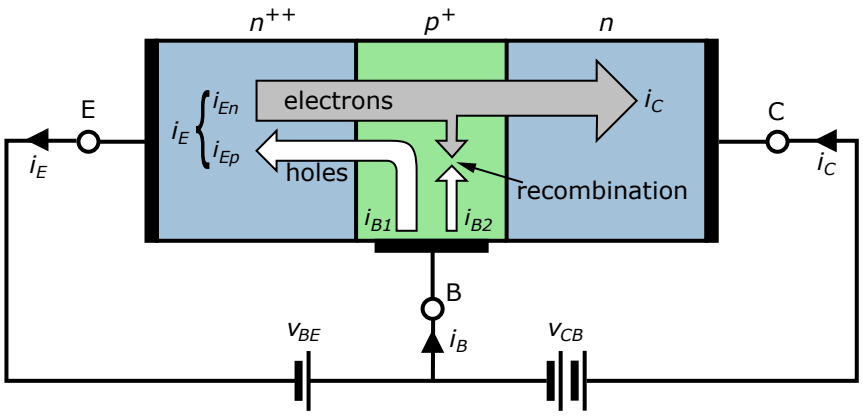


Figure 16: *Cross section of a BJT ([22])*

Figure 16 shows an overview of the BJT transistor, which is the parasitic transistor which exists in the N-Type Metal-Oxide Semiconductor (NMOS) and should help to imagine the snapback effect.
Figure 17 shows on the left an NMOS transistor with its parasitic BJT transistor and on the right the I-V characteristic of it.

3.18.4 | Latchup

Latchup is a phenomena that occurs in the CMOS technology and is mostly unwanted. It can happen due to various reason, whereby the most common is injecting a current into its gate (G1 or G2 from Figure 18).

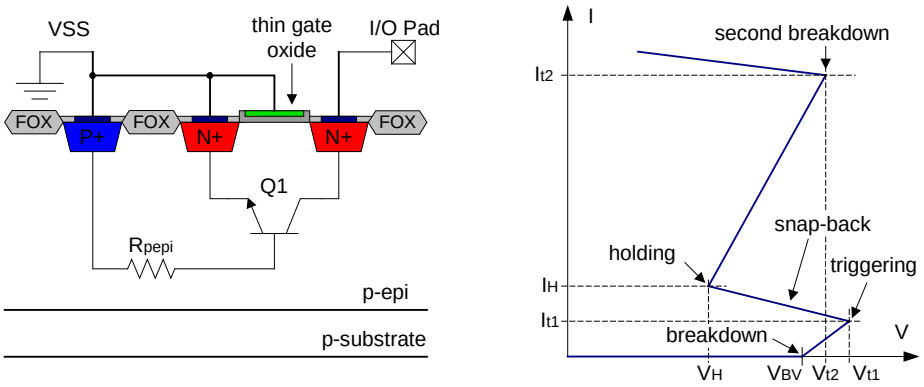


Figure 17: *Cross section of a Gate-Ground-NMOS (GgNMOS) and I-V characteristic ([20] p.28)*

In Figure 18 one can see the the NMOS on the left side and the PMOS in the n-well on the right side. Furthermore one sees the parasitic pnp BJT on the left and the npn BJT on the right side. From Figure 18 one can then extract Figure 19. Whereby R1 is the resistance of the substrate and R2 the resistance of the n-well. Figure 19 also shows that a CMOS forms a Silicon Controlled Rectifier (SCR) [20] [23].
A good video with an explanation can be found under the following link[2].

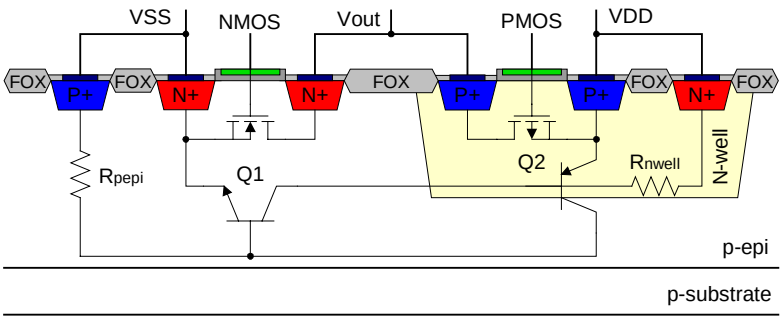


Figure 18: *Cross section of a CMOS output buffer and parasitic components ([20] p.60)*

3.18.5 | Thyristor

A thyristor is also called SCR and acts as a bistable switch/latch, conducting when the gate receives a current trigger, and continuing to conduct until the voltage across the device is reversed biased, or until the voltage is removed [24].

3.18.6 | Latchup Snapback

The literature study has show that it is very common to implement a snapback ESD protection with a GgNMOS on all output pins. Furthermore the large transistors which were used in the design could be modified according to the recommendations given in ([20] p.28 bottom) to have the snapback already implemented.

[2] https://youtu.be/EYHFLBI5fjg

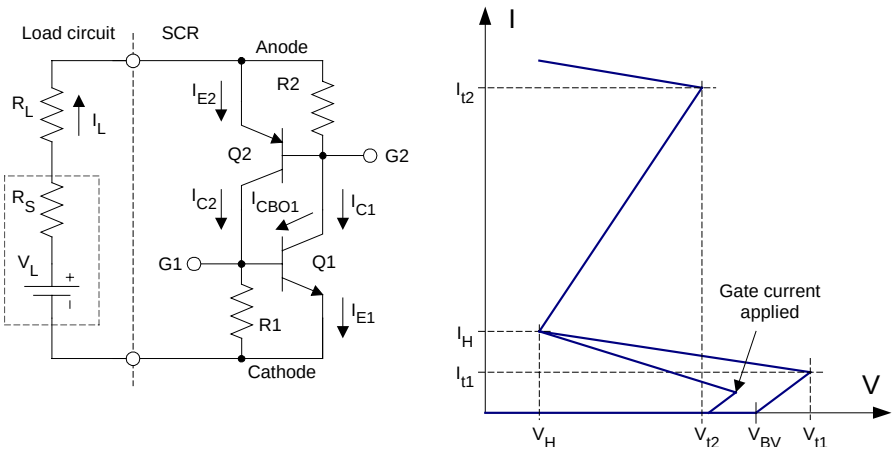


Figure 19: *Bipolar model of a SCR circuit and I-V characteristic ([20] p.69)*

4 | Implementation

In this chapter we will focus on actual implementation of many of the concepts discussed in the previous chapter. The goal is to describe the inner workings of the chip on a conceptual level as well as in a second step the workings of the individual sub-circuits. In a first subchapter we will explore how the control loop was design from a high level perspective. Especially the high-level workings of the controller, some of the problems we encountered and how we over came them. In the second part we will have a detailed look into the underlying sub-circuits that make up the chip and will have a detailed look into design decisions at a single transistor level.

4.1 | High-Level Regulator Design

In this subchapter we will give a look in to the design of the control loop on a high level, without getting caught up with the details of the analog circuits. We will try to explain the reasons behind our design decisions, why we changed the controller topology late in the design process and how the converter works. All sub circuits can generally be considered ideal in this subsection with occasional references to the ruff underlying implementation considerations where needed.

4.1.1 | Converter Overview

The converter we ended up building is a cascaded buck-boost converter based design. As most other highly integrated buck-boost converters use the converter topology, we felt strongly, that this is the right approach. For the structure of the control loop itself, we opted to use peak current-mode control, but only after first implementing average current-mode control and running into problems. We have also implemented synchronous rectification and are using the $R_{DS,on}$ of our power MOSFETs to measure the current flowing the inductor. To ensure stable operation regardless of the duty-cycle, we implemented a slope compensation circuit. The voltage feedback of the converter is done internally with high impedance resistive voltage dividers. The feedback node is also connected to an external pin, which allows with trimming of the output voltage or to completely overwrite the internal divider with a lower impedance external one. This also allows for external compensation of the feedback loop if required. The regulator uses peak current-mode control is implemented using a low g_m Operational Transconductance Amplifier (OTA) with an internal type-II compensation network. The goal is to have bandwidth of 30 kHz while maintaining a phase margin of 60°. For external components we only need a 10 µF input capacitor C_i, a 20 µF output capacitor C_o and a 47 µH external inductor.

4.1.2 | Loop Compensation for Average Current-Mode Control

As we first built the a controller on the average current approach, we designed loop compensation based on the modelling provided by [10]. Based on the modelling provided in the book, we created MATLAB script, which allowed us to quickly model the loop behavior based on various variables like output capacitance, loop bandwidth and switching frequency. The script can found in section 11.The script creates a transfer function for every component in the loop and calculates its bode plots. The script takes as an input the

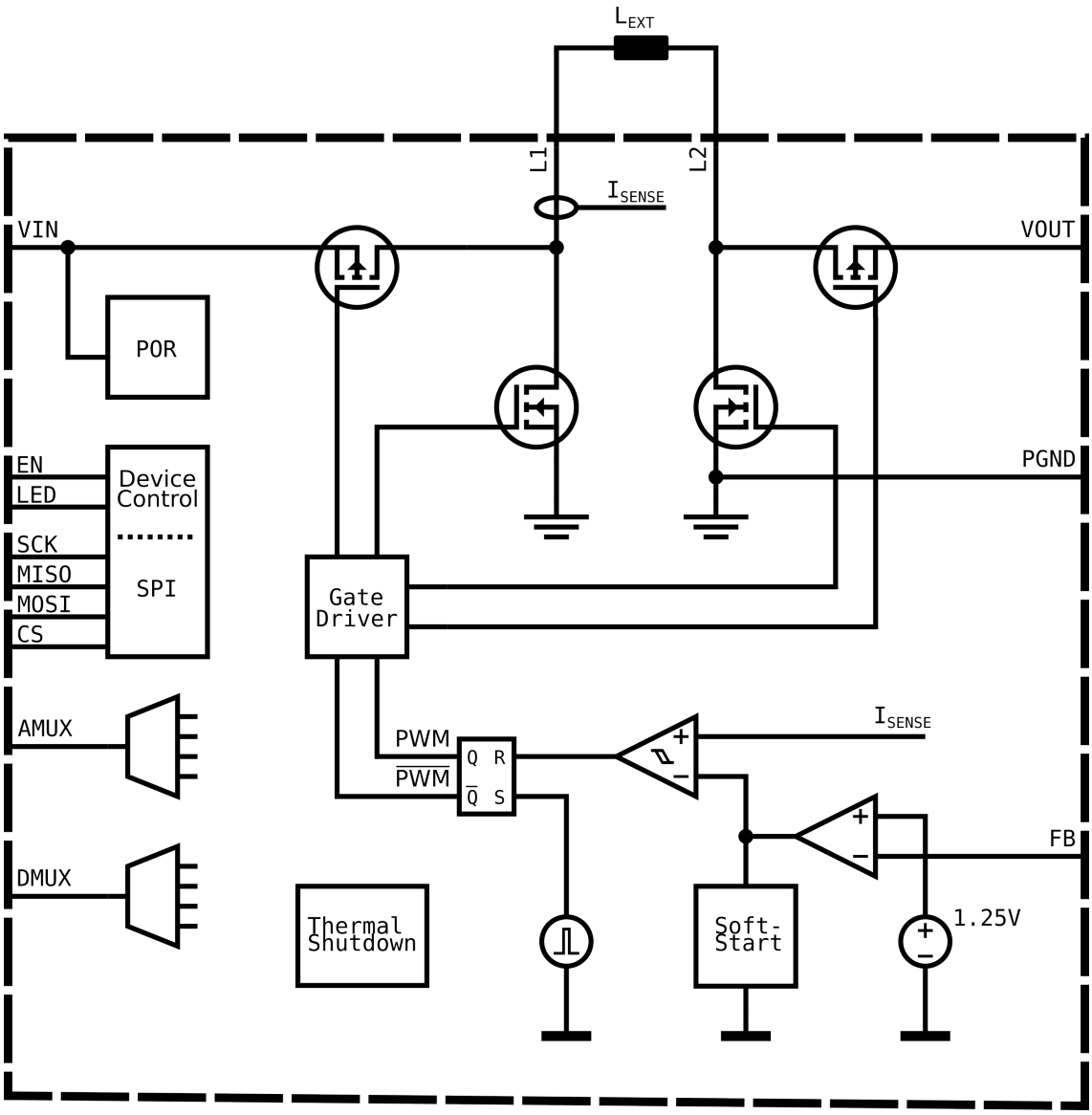


Figure 20: *Functional block diagram of the buck-boost converter*

desired bandwidth and phases of the control loops and calculate the required type-II compensation network. This allowed us to quickly determine which variable constellations lead to a compensation network that is implementable on an IC. We achieved satisfactory results with a 200 kHz RC low-pass filter for the current averaging, 30 kHz current loop bandwidth and 10 kHz voltage loop bandwidth. This was done at a switching frequency of 500 kHz with a 47 µH inductor.

4.1.3 | Issue with Average Current-Mode Control

When we switched out our ideal current measurement for the SenseFET based implementation at transistor level, the regulation behavior became discontinuous for small loads. The problem caused by the inability for the circuit to sense negative currents. With small loads the regulator would normally be operating in Discontinous Conduction Mode (DCM). As we are using synchronous rectification instead of conventional diodes, we are not operating in DCM but always in Continous Conduction Mode (CCM)

as we do not explicitly prevent reverse current flow. In CCM the current in the inductor has a triangular shape oscillating from some minimum to some maximum around the average DC current value. When small loads are applied, the average current is close to 0 A, leading to 50 % of the current to be positive with the other 50 % to be negative. The problem becomes exacerbated as soon as the inductor current starts oscillating, as control loop has no feedback in the time the inductor current is negative. The voltage loop increases the required current continually and the current loop follows, but it only is able to measure the real current flowing in the inductor when it becomes significantly positive, thus leading to an overshoot. This behavior can be seen in Figure 21, the legend is as follows: output voltage, inductor current, output of the outer control loop, measured output current.

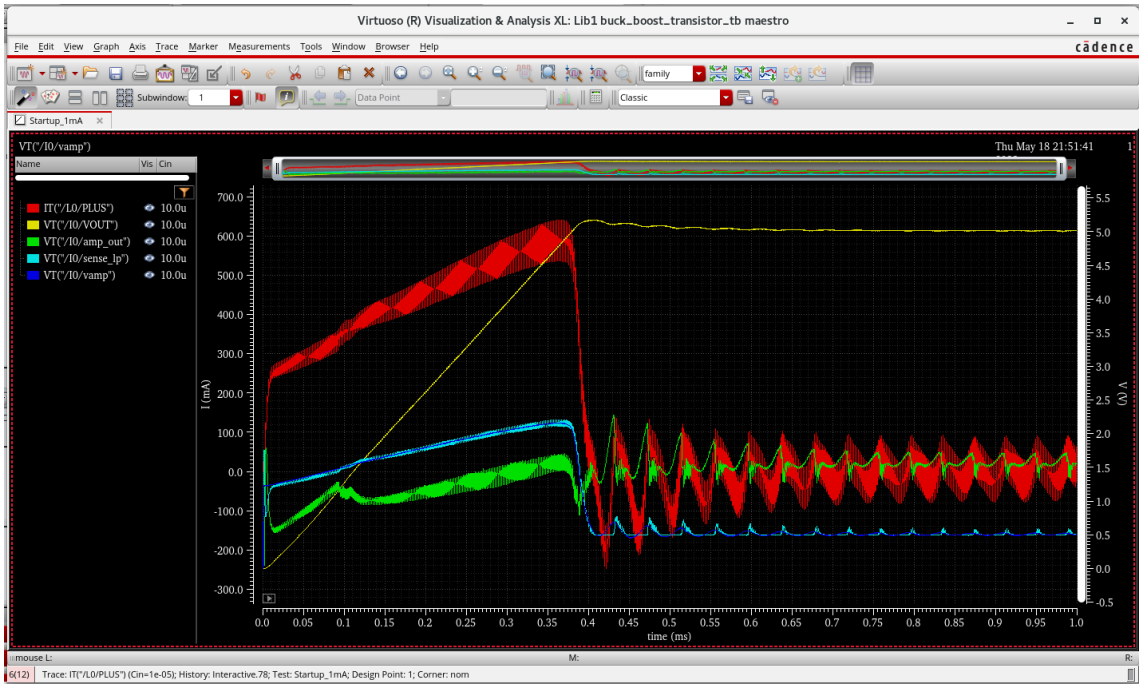


Figure 21: *Oscillating behavior of the average current-mode controller after starting up with a small load*

4.1.4 | Loop Compensation for Peak Current-Mode Control

The implementation of the regulator peak current-mode control was conducted similar to the one already done with average current-mode control. As basis we took the calculations and modelling from [12]. The script can found in section 11. We once again created MATLAB script to do all the calculations an plotting. After running some simulations based on the values from the script, we noticed a large current ripple in the inductor of about 100 mA. Instead of further increasing the inductors size, we would increase the switching frequency to 1 MHz. We settled on the value of a 30 kHz bandwidth and 60° phase margin as it leads to good regulation characteristics, while requiring a compensation network that is manufacturable on a chip.

4.1.5 | Protection Features

Lastly we implemented various protection features. The first of which is the inductor current limit. The inductor current has hard limit implemented of around 600 mA. This limit is dependent on the current duty-cycle, as the slope compensation interferes with it. Additionally we implemented another inductor current limit, which is dependent on the output voltage. The current limit is lower then the other limit at output voltages lower then 1.2 V. This current limit is proportional to the output voltage and limits to inductor current to less then 300 mA if the output is shorted to GND. The entire current limiting circuit behaves therefore as a constant current source under light overload conditions, but has foldback behavior if the load is significantly to high.
As we are potentially generating a lot of heat in the power transistors, we implemented an over-temperature protection circuit. This circuit should be placed close to the switching transistors and disables the converter if the temperature fo the chip exceeds a threshold. This thermal shutdown circuit also has hysteresis to prevent the converter from quickly turning on and off again if it reaches the temperature threshold.

4.2 | Implementation of Transistor-Level Circuits

Upon completion of the literature research, a comprehensive understanding of the required components and their functionalities was gained. Utilizing a top-down approach, the design of the ASIC commenced, wherein the different functionalities were divided into distinct blocks, as depicted in Figure 22. Initially, these blocks were implemented at a high abstraction level, and subsequently, in greater detail at the semiconductor level. This subsection provides an overview and description of each individual block, shedding light on their specific roles and characteristics.

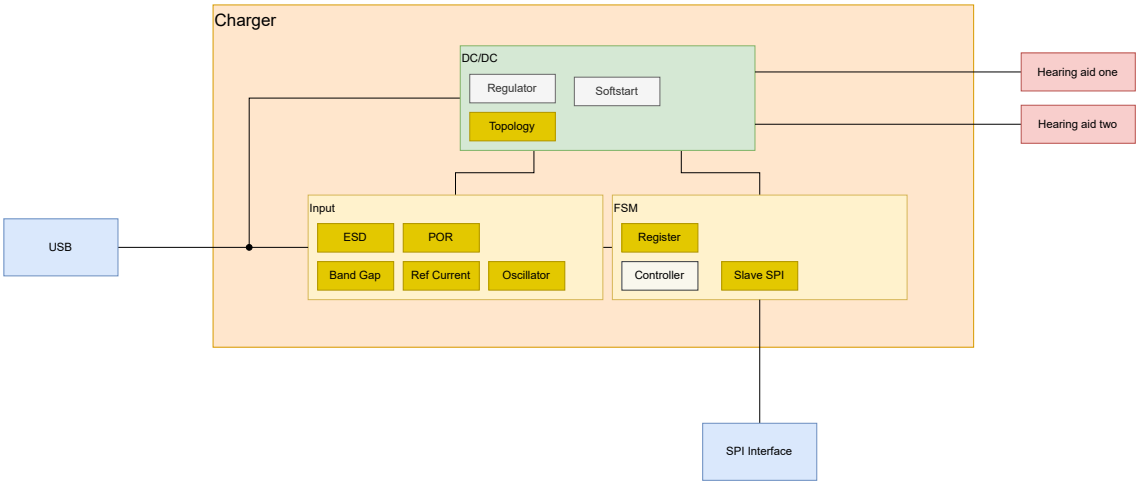


Figure 22: *Our implementation of cascaded Buck Boost converter with active switches instead of diodes*

4.2.1 | Simulations

For all the blocks mentioned in this subsection corner and Monte Carlo simulations were executed with the parameters mentioned below, when not otherwise mentioned. Thereby

the shortcuts have the following meaning (further explanation can be found in Table 7 and ([25] p.7)):

tm → **t**ypical **m**ean
wp → **w**orst case **p**ower
ws → **w**orst case **s**peed
wo → **w**orst case **o**ne
wz → **w**orst case **z**ero

Model Class	Parameter	wp	ws	wo	wz
MOS	NMOS	fast	slow	fast	slow
	PMOS	fast	slow	slow	fast
Bipolar Transistors	speed	high	low	-	-
	beta	high	low	-	-
Capacitors	capacitance	low	high	-	-
Varactors	capacitance	low	high	-	-

Table 7: *parameter mix in predefined X-FAB corners [25]*

4.2.1.1 | Corner Simulations

param.scs= 3s
xh035.scs=wo wz ws wp
Vdd=4.3 5 5.5
Temperature=0 70

4.2.1.2 | Monte Carlo Simulation

param.scs= 3s
xh035.scs=mc_g

4.2.2 | Input

The input block includes a POR circuit which makes sure that the circuit turns only on when the input voltage reaches a certain level, a current reference which provides an input voltage and more or less temperature independent current source, a bandgap reference which provides a input voltage and temperature independent voltage reference and an oscillator which provides a clock for the FSM.

4.2.2.1 | Current Source

Having a power supply (input voltage) independent current source is one of the key functionality for this project. Due to the fact that current sources are needed for multiple amplifier circuits which are included in function blocks such as the bandgap reference.
Since this problem was solved already multiple times before it was decided to go with a pre-existing solution/schematic as already mentioned in section 3. Lars Kamm therefore provided us with such a circuit, which was afterwards slightly adapted and will be discussed in this section.

Circuit At first glance comprehending a circuit like the one depicted in Figure 28 may present some difficulties. Therefore, the following section provides a step-by-step description of the circuit.

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \underbrace{(1 + \lambda V_{DS})}_{\text{Can be neglected for simplicity}} \tag{2}$$

$$\Delta V_{GS} = V_{GS} - V_T \tag{3}$$

$$\Delta V_{GS} = \sqrt{\frac{I_0}{\frac{\mu \cdot C_{ox}}{2} \frac{W}{L}}} \tag{4}$$

The concept behind the current reference circuit is to leverage the threshold voltage (V_T) of the MOSFET, as this parameter remains unaffected by the supply voltage, as indicated in Equation 2, which shows the current through a MOSFET in saturation region. To fully comprehend the circuit in Figure 26, it is essential to grasp basic circuits such as the one shown in Figure 23. In this particular circuit, the voltage at the gate of M_0 is zero, resulting in the absence of a voltage V_T anywhere. In order to establish the desired voltage V_T across the transistor, a certain current i_D must flow. Achieving this can be accomplished by introducing a current mirror into the circuit. When doing that one ends up with Figure 24.

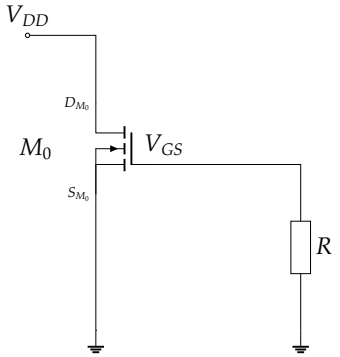


Figure 23: *Current reference intro*

In Figure 24 one has on the gate of M_0 the voltage $\Delta V_{GS} + V_T$ whereby $\Delta V_{GS} = V_{GS} - V_T$ as indicated in Equation 3. When one now increases the ratio of $\frac{W}{L}$ ΔV_{GS} decreases as one can see from Equation 4, which says: $\Delta V_{GS} = \sqrt{\frac{I_0}{\frac{\mu \cdot C_{ox}}{2} \frac{W}{L}}}$. Therefore when the ratio $\frac{W}{L}$ goes to infinity one would have a stable current through R and a stable voltage on the gate of M_0, when one does not consider that V_T is dependent on the temperature and the process. But the issue with the circuit in Figure 24 is that one has a positive feedback loop, which means when the gate voltage on M_0 increases the current on M_1 and M_2 increases too, which increases the gate voltage of M_0 even more ($\Rightarrow$ Circuit is unstable). To prevent that one would need to insert an additional MOSFET below M_2. But as one can see from this circuit one is still dependent on V_{GS} when the ratio of $\frac{W}{L}$ is not infinity. Let's therefore see if it gets better when one makes sure that the voltage is the same on the gate and the drain of M_0. One achieves this with the circuit in Figure 25. The gate voltage of M_0 is

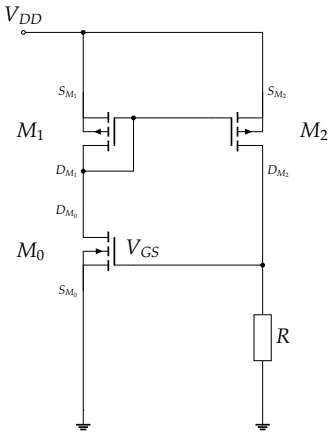


Figure 24: *Current reference example one*

$\Delta V_{GS} + V_T$ and on M_3 and M_4 $2 \cdot \Delta V_{GS} + 2 \cdot V_T$. Therefore the voltage over R is $\Delta V_{GS} + V_T$. But when one decreases the ratio of $\frac{W}{L}$ of M_4 by a factor of 4 the voltage over R reduces to V_T which means one gets rid of ΔV_{GS} and should therefore be completely independent of V_{DD} [26]. When one tries to control the temperature dependency too one could add

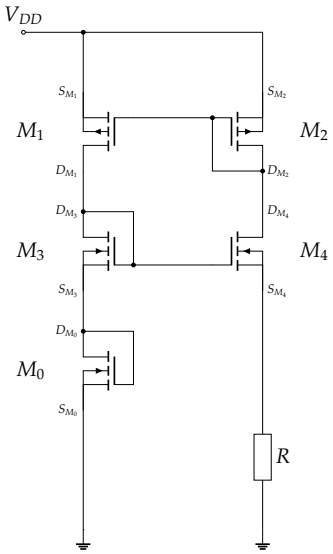


Figure 25: *Current reference example two*

an additional NMOS (M_5) above R with a $\frac{W}{L}$ x times larger than the one from M_0, as it can be seen in Figure 26. Since one knows that the voltage and the current on the source of M_3 and M_4 is the same one can write the following equations:

$$\begin{aligned} I_R &= \frac{U_R}{R} \\ I_{S_{M_0}} &= I_{S_{M_5}} \\ \sqrt{\frac{I_{S_{M_0}}}{\frac{\mu \cdot C_{ox}}{2} \frac{W}{L}(1 + \lambda V_{DS})}} + V_T &= \sqrt{\frac{I_{S_{M_5}}}{\frac{\mu \cdot C_{ox}}{2} \frac{W}{L}(1 + \lambda V_{DS}) \cdot x}} + V_T + U_r \end{aligned} \tag{5}$$

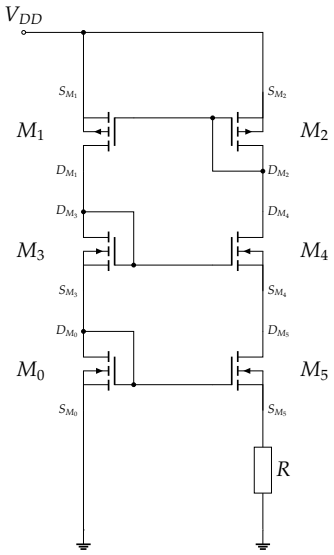


Figure 26: *Current reference*

whereby:

$$\beta_0 = \mu_n C_{ox} \tag{6}$$

$$\beta = \frac{W}{L} \cdot \beta_0 \tag{7}$$

- x: factor $\frac{W}{L}$ of M_5 is larger than M_0
- U_R: Voltage over resistor
- β: Transconductance Parameter
- W: Width of the MOSFET
- L: Length of the MOSFET
- μ_n: Mobility of an electron $\propto \frac{1}{T}$
- C_{ox}: Capacitance per unit area of the oxide = $\frac{t_{ox}}{\epsilon_{os}}$

The result of Equation 5 is then (when one neglects the trivial solution where $I_{S_{M_0}} = I_{S_{M_5}} = 0$ and the channel length modulation):

$$I_{S_{M_0}} = I_{S_{M_5}} = \frac{2 \cdot (x \pm 2\sqrt{x} + 1)}{\beta_0 \cdot \frac{W}{L} \cdot R^2 \cdot x} \text{ !}$$

$$U_R = \frac{2 \cdot (x \pm 2\sqrt{x} + 1)}{\beta_0 \cdot \frac{W}{L} \cdot R \cdot x} \text{ !}$$

One solution from the equations above is an extraneous solutions. The solutions that are really correct are: $I_{S_{M_0}} = I_{S_{M_5}} = \frac{2\cdot(x-2\sqrt{x}+1)}{\beta_0 \cdot \frac{W}{L} \cdot R^2 \cdot x}$ and $U_R = \frac{2\cdot(x-2\sqrt{x}+1)}{\beta_0 \cdot \frac{W}{L} \cdot R \cdot x}$. As one can see from those equations the current is depending on the factor of x and R one can therefore set it with setting x and R respectively. Furthermore it is worth to mention that R has a positive temperature coefficient and V_{GS} a negative one. Therefore when the temperature increases the resistance R gets higher while V_{GS} gets lower. Due to that one could chose R and x in such a way that the circuit is more or less temperature independent. Due to the fact the amplifiers in the other circuits are also temperature

dependent one chooses the ratio in such a way the the amplifiers are in the end not temperature dependent. But since this goes really deep into semiconductor physics no formulas for the temperature dependency of this circuits were derived. Nevertheless the simulation results were verified with the temperature independent equations which have shown that the calculations and simulations are quite similar.
When inserting the values of the circuit one gets the following result:

$$I_{S_{M_0}} = I_{S_{M_5}} = \frac{2 \cdot \left(16 - 2\sqrt{16} + 1\right)}{103 \times 10^{-6}\,\mathrm{A\,V^{-2}} \cdot 16 \cdot 22.5 \times 10^{-3}\,\Omega^2 \cdot 16} = 2.697 \times 10^{-6}\,\mathrm{A}$$

$$U_R = \frac{2 \cdot \left(16 - 2\sqrt{16} + 1\right)}{103 \times 10^{-6}\,\mathrm{A\,V^{-2}} \cdot 16 \cdot 22.5 \times 10^{-3}\,\Omega \cdot 16} = 168.554\,\mathrm{mV}$$

with:

β	$103\,\mu\mathrm{A\,V^{-2}}$
R	$22.5\,\mathrm{k\Omega}$
$\frac{W}{L}$	8
x	16

This similar to the simulation (simulation[3]: 4.9 µA, calculation: 2.7 µA).

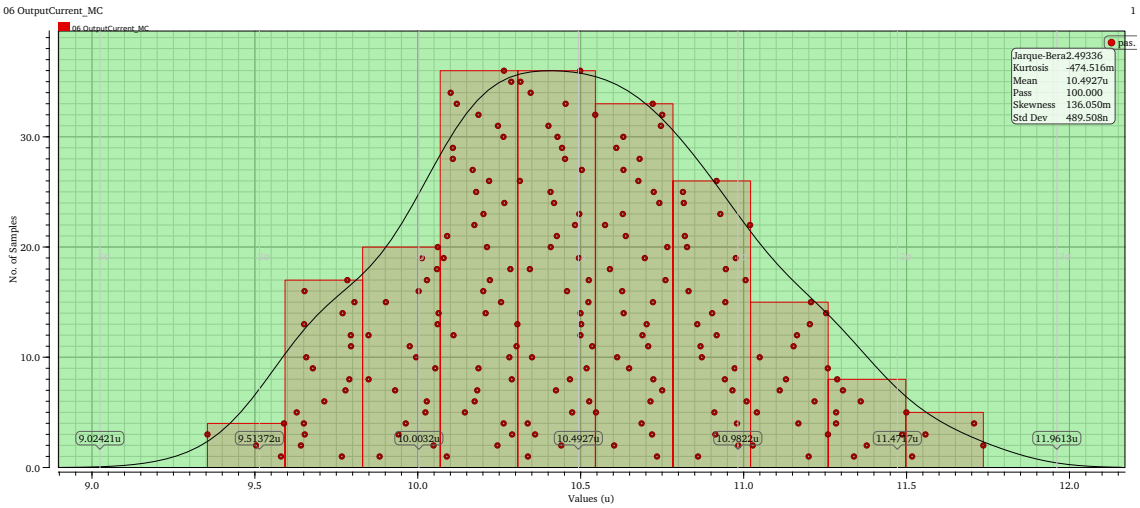


Figure 27: *Monte Carlo distribution of Current reference. X-axis shows current through „IPRB0" in Figure 29 (param.scs=3s, xh035.scs=mcg)*

The implemented design on the chip can be seen in Figure 28. For simplicity one can neglect in a first step M89, M10, M13, M19 and M21. When doing that one sees in Figure 28 the same circuit as in Figure 26 with some additions (M51 and M52 are not needed they were introduced in the layout for a common centroid design). This additions are needed since one has two operating points as one saw before. To be in the right operating point a so called start up circuit is needed which will be explained in more detail. On the left of Figure 28 one finds the enable signal EN and its inverted signal ENN. In turned

[3] Simulation result can be found in Figure 74 in the appendix

off state M15 is conducting an therefore M14 discharged, furthermore VB4 is pulled to VDDA which forces the bootstrap to be in state zero (state where no current is flowing). When the circuit is turned on M8, M9 and M11 are conducting, since their gate voltage is zero which leads to the fact that the node voltage of N2 is pulled to VDDA. Furthermore VB4 is not any more pulled to VDDA. The voltage in N2 causes a current in the current reference which is mirrored to M5, which charges the capacitor M14 and finally stops N2 to be pulled to VDDA. The current reference is now in its operating state where current is flowing. This current can then be further mirrored to other components with VB4, VB3, VB2 and VB1. Figure 29 shows the testbench used to test the current reference circuit.

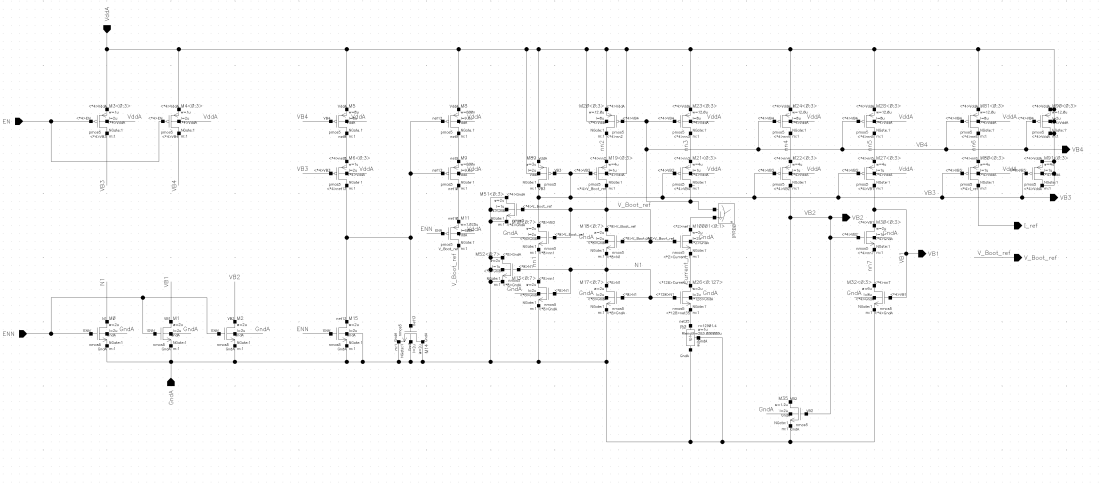


Figure 28: *Current reference Implemented*

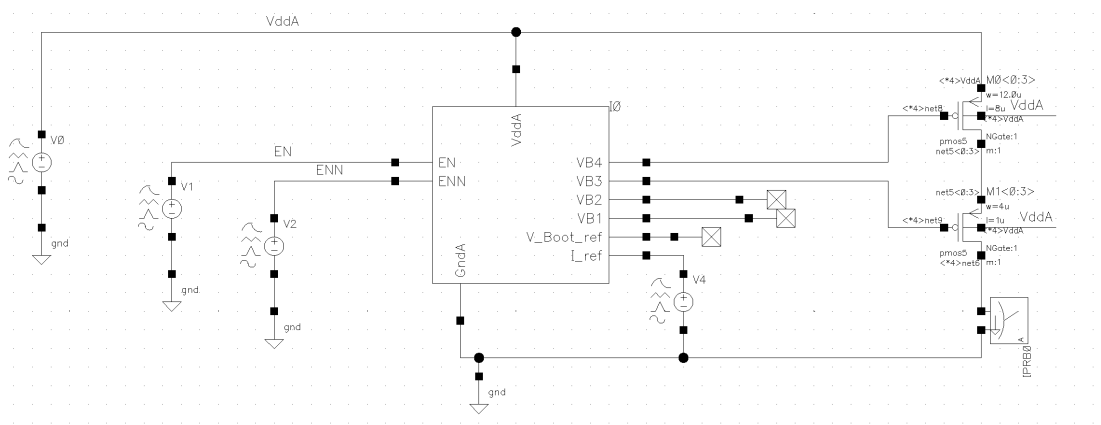


Figure 29: *Current reference test bench*

Figure 30 shows the current in dependency of the supply voltage. Figure 31 shows the transresistance of the input voltage to the output current. It is visible from this plot that the current reference should be operated with a voltage greater than 3.3V to have a input voltage independent current.

Figure 32 shows the output resistance of the current reference (V_4 in Figure 29) divided by the current that goes into the source of V_4 at different voltages. This allows to estimate

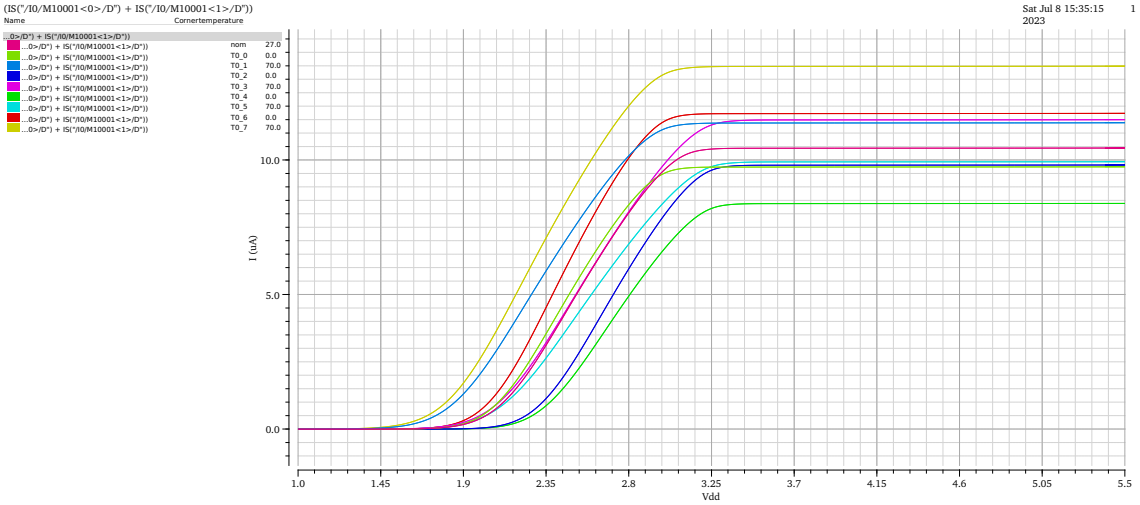


Figure 30: *Current reference current vs supply voltage*

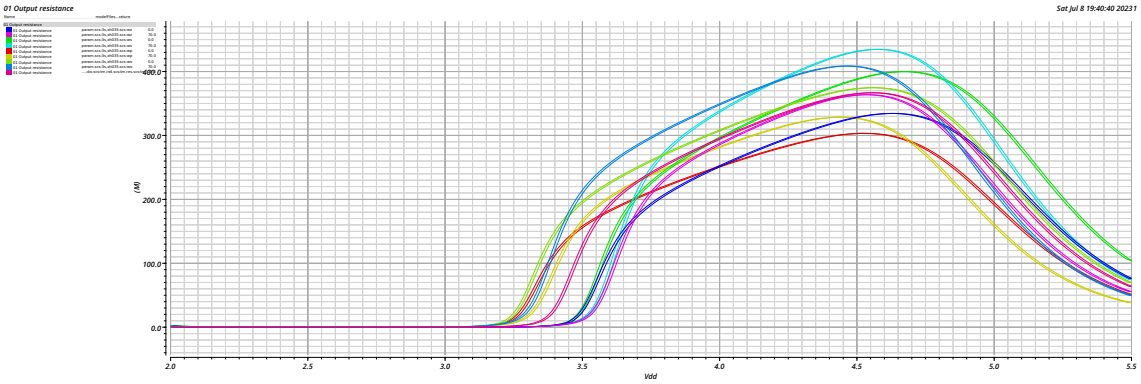


Figure 31: *Current reference trans resistance* $\frac{\Delta V_{in}}{\Delta I_{out}}$

how many diode voltage one is allowed to use to mirror the reference current. It shows that the voltage of the diode must be at least 0.8V below the supply voltage.
The summarized specification of the block can be found in Table 8.

Description	Min	Max	Unit
Reference current	8.4	13.5	µA
Current consumption	50	81	µA
Min voltage (voltage where the trans resistance ($\frac{\Delta V_{in}}{\Delta I_{out}}$) is higher than 1 MΩ)	3	3.33	V

Table 8: *Current reference characteristics*

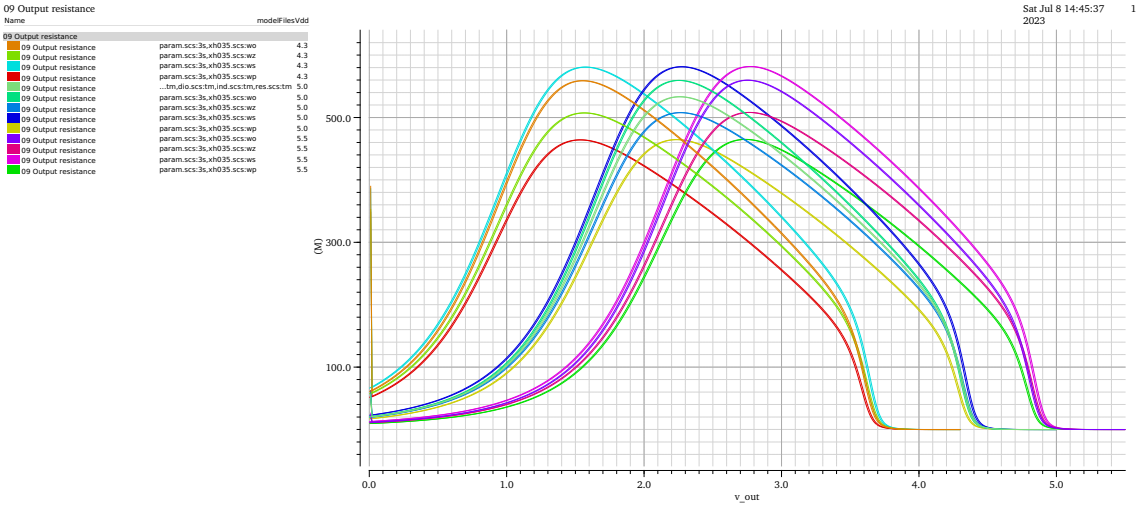


Figure 32: *Current reference output resistance* $\frac{\Delta V_{out}}{\Delta I_{out}}$

4.2.2.2 | Bandgap

For the Bandgap reference a given implementation of a 3.3 V circuit from X-Fab was taken and adapted for the 5 V technology as mentioned in section 2. The final design can be seen in Figure 33.

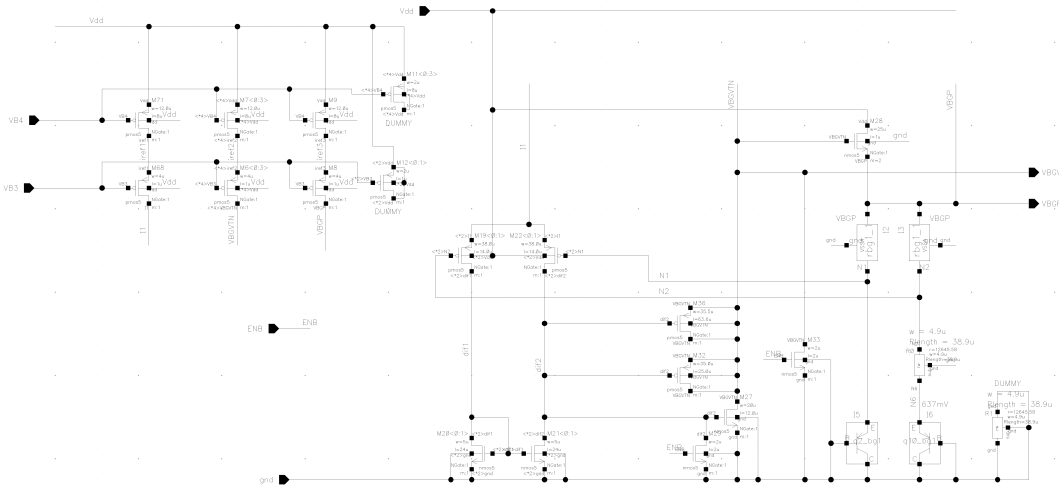


Figure 33: *Bandgap schematic*

For the test the schematic in Figure 34 was used, where EN is set to 5 V and ENN to 0 V furthermore VDDA was sweept from 0 V to 5.5 V

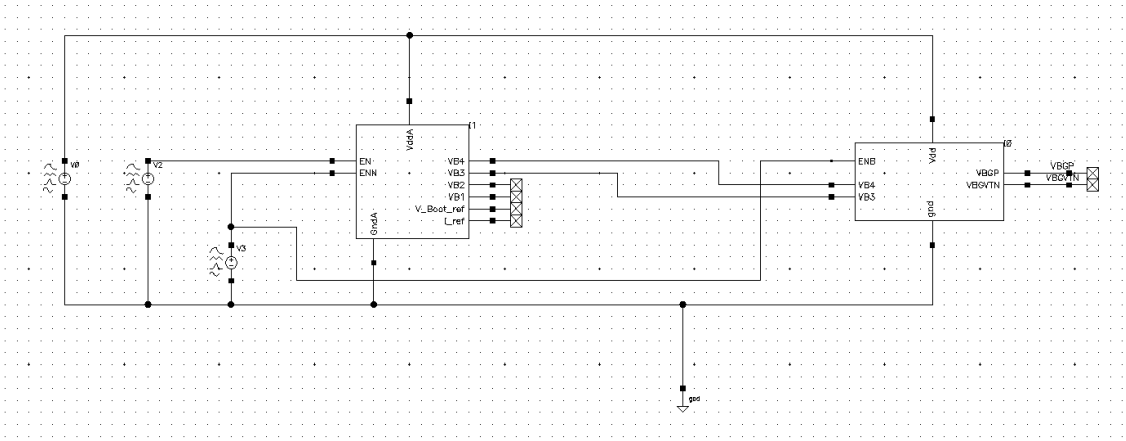


Figure 34: *Bandgap testbench*

Figure 35 shows that the bandgap voltage is quite stable over the corners, but slight variations can be seen in Figure 36 the Monte Carlo simulation. But since the exact output voltage of the DC/DC converter can be exactly set by a external resistor the variance over the temperature and supply voltage plays a major role. Which is very low as can be seen in Figure 35 and Figure 37.
Figure 37 shows the dependency of the bandgap voltage vs the temperature.
Table 9 Show the characteristics of the bandgap design used in this project.

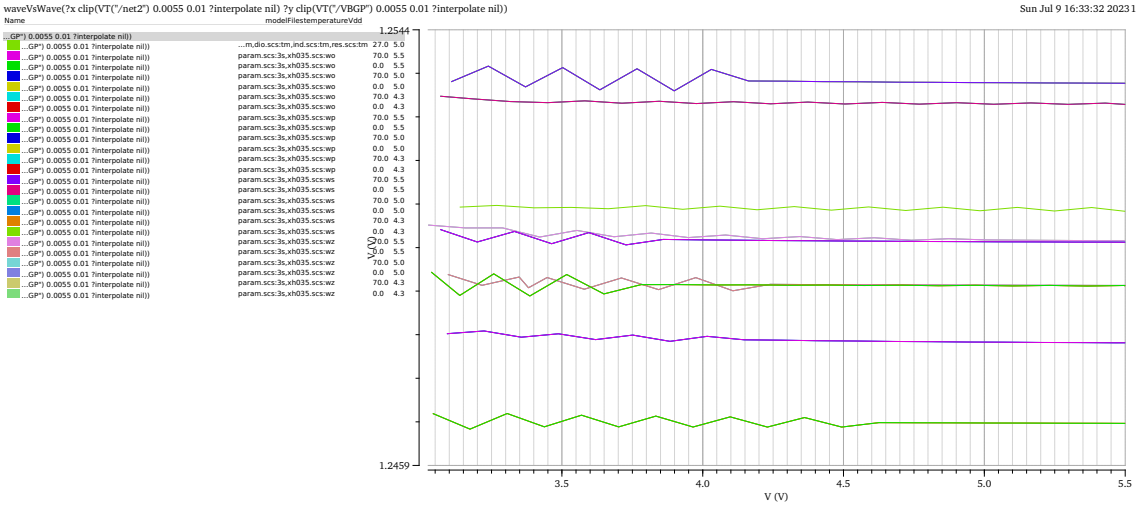


Figure 35: *Bandgap voltage vs supply voltage*

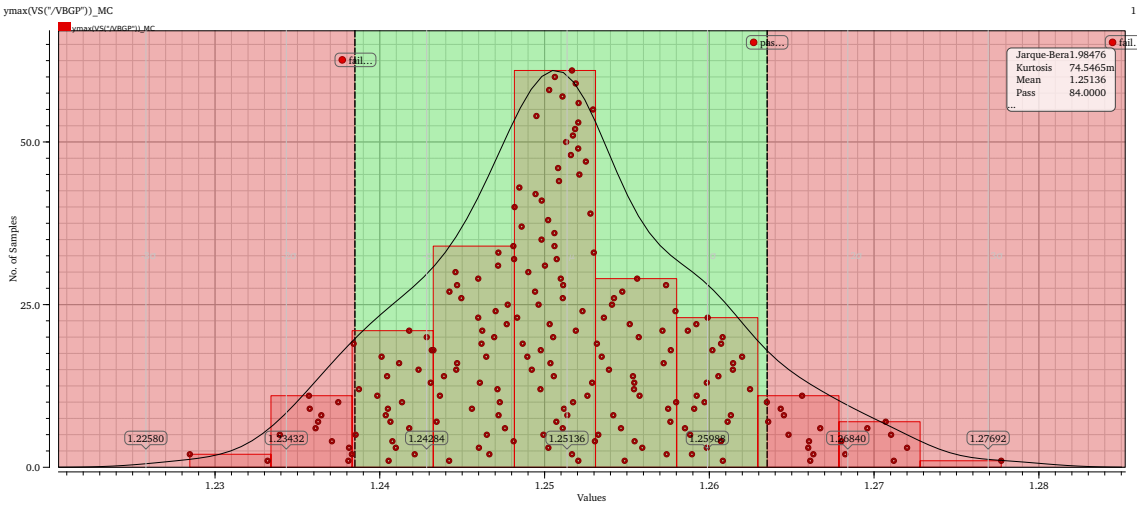


Figure 36: *Bandgap voltage Monte Carlo simulation (param.scs=3s, xh035.scs=mcg)*

Description	Min	Max	Unit
Bandgap voltage	1.226	1.277	V
Current consumption	16.73	23.53	µA
Min voltage	2.3	2.9	V

Table 9: *Bandgap characteristic*

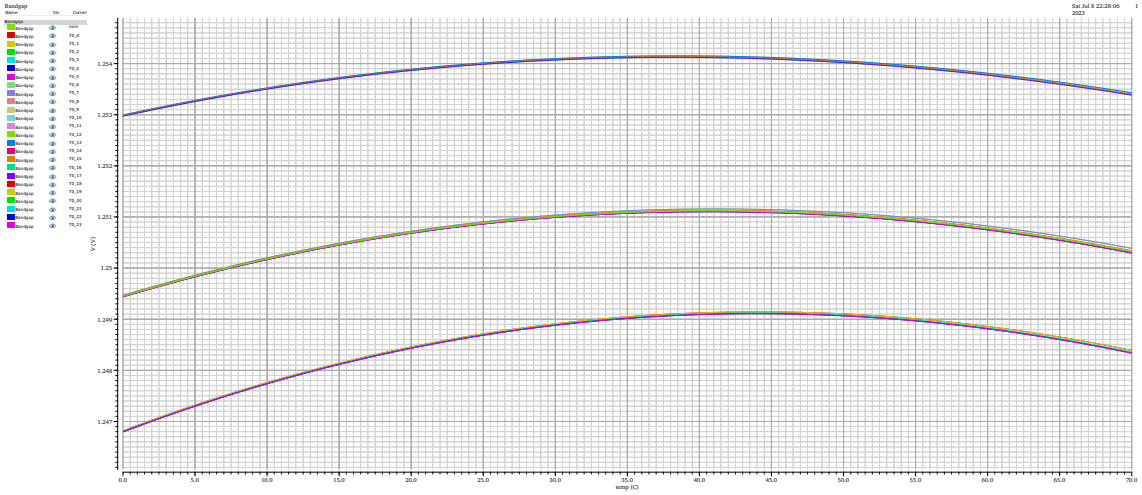


Figure 37: *Bandgap voltage vs temperature*

4.2.2.3 | Oscillator

For the digital part of the circuit there is a clock required to process the data received over the SPI. [4] Since the SPI standard does not define a certain clock speed the frequency generated in the ASIC plays a minor role. Due to that it was decided to generate the clock with a sawtooth generator (a capacitor gets charged with a certain current and as soon as it reaches a threshold it gets discharged) due to the fact that this approach is very easy to implement and fully compatible with the CMOS process used.
Since also the DC/DC converter uses a sawtooth generator with some additions (slope compensation) it was not yet decided which design is used in the final ASIC. What is already sure is that one wants to use in both designs the same topology since then only the capacitor size has to be changed and one can use the same layout. Due to that no concrete layout is mentioned here, but when one would use a very simple sawtooth generator one would reach the specs which are listed in Table 10. To compensate the large variation in frequency it is planned to make the capacitor which determines the frequency configurable over the SPI interface with three switches, which means one can configure 8 different frequencies/capacitance values. The most important values can be read from Table 10.

Description	Min	Max	Unit
Frequency	1.15	1.7	MHz
Current consumption	35	50	µA
Min voltage	2	3.187	V

Table 10: *Specification*

[4] It was decided to generate an internal clock although it would have been possible to build a finite state machine which uses the SPI signal only to read and write the registers.

4.2.2.4 | POR

For the POR circuit an example was provided by Lars Kamm and afterwards adapted, so that it has the right power on voltage and delay time. The final design can be seen in Figure 38.

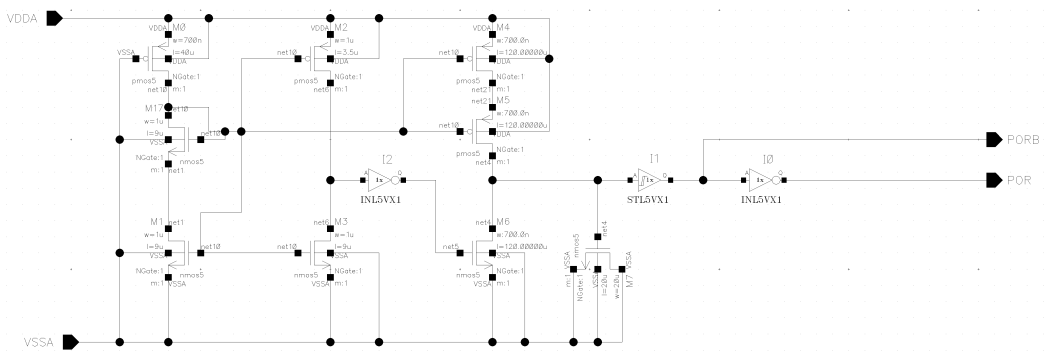


Figure 38: *POR schematic*

The test bench with which the design was tested is visible in Figure 39. In Figure 41 the

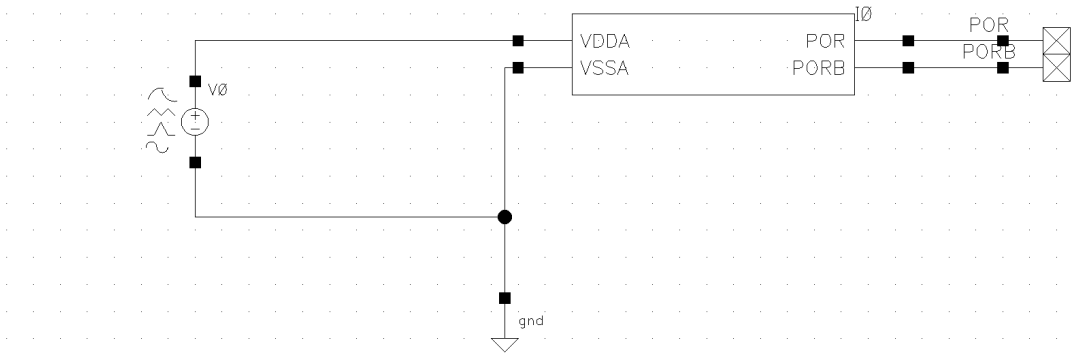


Figure 39: *POR testbench schematic*

test sequence for the delay measurement is visible. In pink one sees the supply voltage and in red the PORB signal. Which is on high when the circuit should work.
Figure 41 show the test output of the test-bench. It's output is summarized in Table 11.

Description	Min	Max	Unit
input delay	26	44	µs
output delay	4.4	6.8	µs
Current consumption	13	31	µA
Min voltage	3.176	3.7	V

Table 11: *POR characteristic*

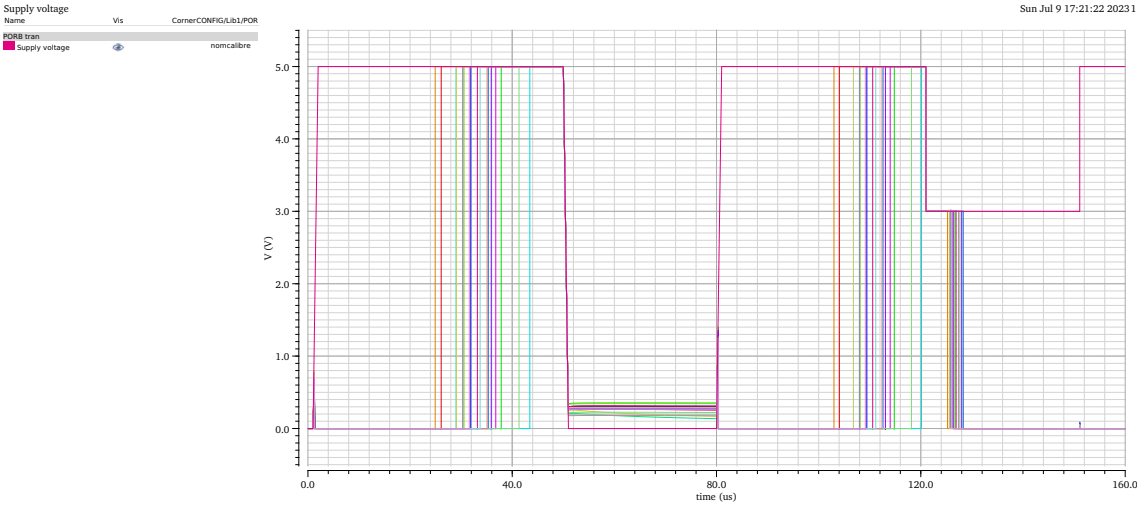
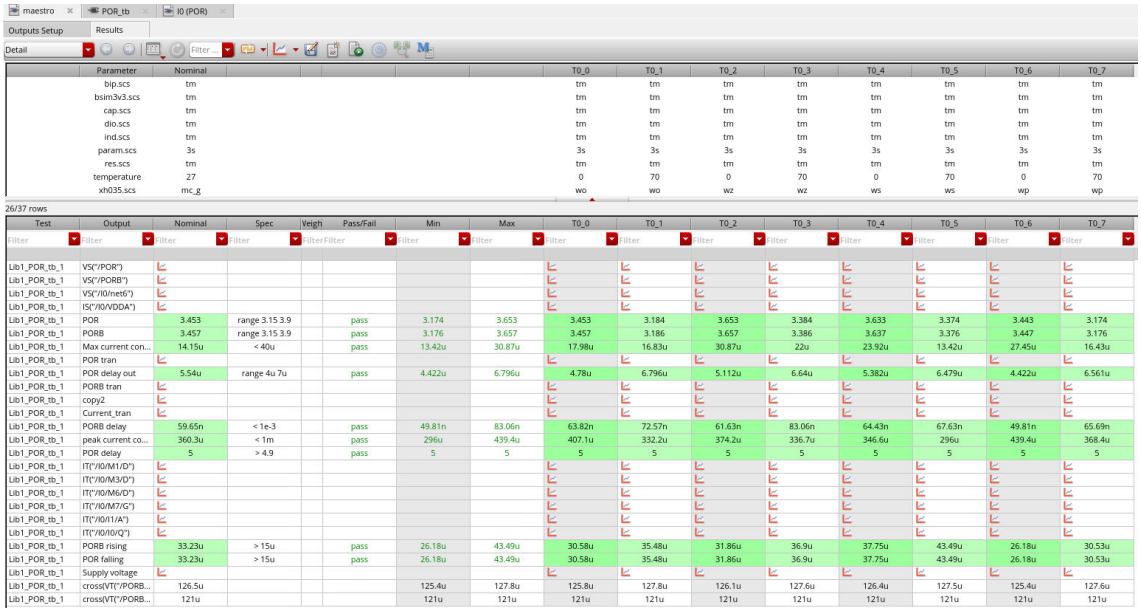


Figure 40: *POR transient simulation*



Parameter	Nominal	T0_0	T0_1	T0_2	T0_3	T0_4	T0_5	T0_6	T0_7
bip.scs	tm	tm	tm	tm	tm	tm	tm	tm	tm
bsim3v3.scs	tm	tm	tm	tm	tm	tm	tm	tm	tm
cap.scs	tm	tm	tm	tm	tm	tm	tm	tm	tm
dio.scs	tm	tm	tm	tm	tm	tm	tm	tm	tm
ind.scs	tm	tm	tm	tm	tm	tm	tm	tm	tm
param.scs	3s	3s	3s	3s	3s	3s	3s	3s	3s
res.scs	tm	tm	tm	tm	tm	tm	tm	tm	tm
temperature	27	0	70	0	70	0	70	0	70
xh035.scs	mc_g	wo	wo	wz	wz	ws	ws	wp	wp

Test	Output	Nominal	Spec	Weigh	Pass/Fail	Min	Max	T0_0	T0_1	T0_2	T0_3	T0_4	T0_5	T0_6	T0_7
Lib1_POR_tb_1	VS("/POR")														
Lib1_POR_tb_1	VS("/PORB")														
Lib1_POR_tb_1	VS("/I0/net6")														
Lib1_POR_tb_1	IS("/I0/VDDA")														
Lib1_POR_tb_1	POR	3.453	range 3.15 3.9		pass	3.174	3.653	3.453	3.184	3.653	3.384	3.633	3.374	3.443	3.174
Lib1_POR_tb_1	PORB	3.457	range 3.15 3.9		pass	3.176	3.657	3.457	3.186	3.657	3.386	3.637	3.376	3.447	3.176
Lib1_POR_tb_1	Max current con...	14.15u	< 40u		pass	13.42u	30.87u	17.98u	16.83u	30.87u	22u	23.92u	13.42u	27.45u	16.43u
Lib1_POR_tb_1	POR tran														
Lib1_POR_tb_1	POR delay out	5.54u	range 4u 7u		pass	4.422u	6.796u	4.78u	6.796u	5.112u	6.64u	5.382u	6.479u	4.422u	6.561u
Lib1_POR_tb_1	PORB tran														
Lib1_POR_tb_1	copy2														
Lib1_POR_tb_1	Current_tran														
Lib1_POR_tb_1	PORB delay	59.65n	< 1e-3		pass	49.81n	83.06n	63.82n	72.57n	61.63n	83.06n	64.43n	67.63n	49.81n	65.69n
Lib1_POR_tb_1	peak current co...	360.3u	< 1m		pass	296u	439.4u	407.1u	332.2u	374.2u	336.7u	346.6u	296u	439.4u	368.4u
Lib1_POR_tb_1	POR delay	5	> 4.9		pass	5	5	5	5	5	5	5	5	5	5
Lib1_POR_tb_1	IT("/I0/M1/D")														
Lib1_POR_tb_1	IT("/I0/M3/D")														
Lib1_POR_tb_1	IT("/I0/M6/D")														
Lib1_POR_tb_1	IT("/I0/M7/G")														
Lib1_POR_tb_1	IT("/I0/I1/A")														
Lib1_POR_tb_1	IT("/I0/I0/Q")														
Lib1_POR_tb_1	PORB rising	33.23u	> 15u		pass	26.18u	43.49u	30.58u	35.48u	31.86u	36.9u	37.75u	43.49u	26.18u	30.53u
Lib1_POR_tb_1	POR falling	33.23u	> 15u		pass	26.18u	43.49u	30.58u	35.48u	31.86u	36.9u	37.75u	43.49u	26.18u	30.53u
Lib1_POR_tb_1	Supply voltage														
Lib1_POR_tb_1	cross(VT("/PORB...	126.5u				125.4u	127.8u	125.8u	127.8u	126.1u	127.6u	126.4u	127.5u	125.4u	127.6u
Lib1_POR_tb_1	cross(VT("/PORB...	121u				121u	121u	121u	121u	121u	121u	121u	121u	121u	121u

Figure 41: *POR test output*

4.2.2.5 | Conclusion Input Blocks

As seen in the previous section, we have successfully designed, simulated, and tested all the input blocks. While a comprehensive explanation of the current reference circuit was provided, we have not delved into the same level of detail for the other blocks. This is because these blocks are less complex and are already well-documented in publicly available resources. Additionally, for the reader, the precise implementation and calculations may not be crucial. The simulation results hold greater significance since they utilize more accurate transistor models compared to our manual calculations. Nonetheless, manual analysis and understanding of the circuits underlying concepts remain helpful in conjunction with the simulation results.

4.2.3 | Pads

In order to achieve the required 200 mA output, it became apparent that a single pad per input and output on the ASIC is insufficient to handle such high currents. According to the data sheet, each pad can handle up to 50 mA. As a result, it was decided to utilize a chip with 48 pads, distributed evenly with 12 on each side. This arrangement allows that the Inductor, hearing instruments, GND and VDD pad have multiple pads.
Referring to Table 12, it is evident that 40 pads are definitely necessary, and an additional 8 pads remain unassigned but could potentially be utilized in the layout phase to further decrease the input resistance of the high current connections. According to ([27] p.292)

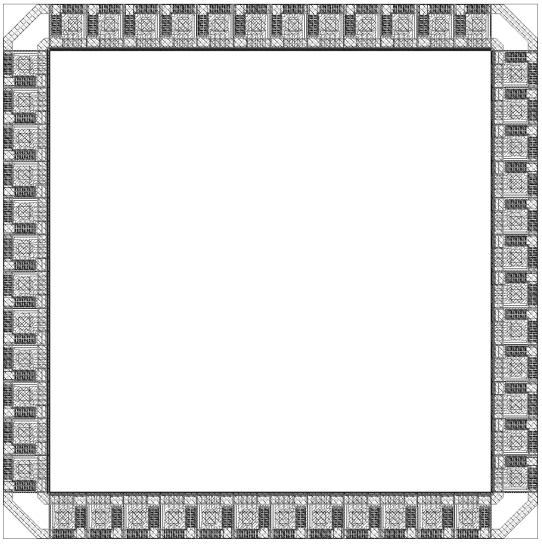
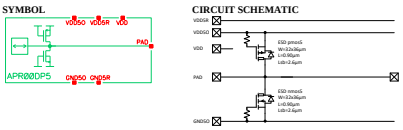
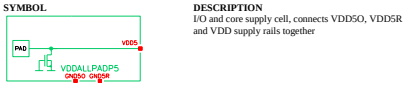


Figure 42: *Pad ring*

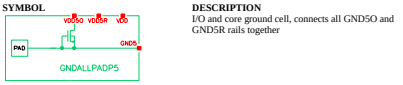
the cell size for a pad limited chip is about 321 µm times 62 µm and for a core limited chip about 210 µm times 216 µm. Since we need huge transistors in our design to switch the current we will use core limited pads as it can be seen in Figure 42. The exact name and schematic of the pads used can be seen in Figure 43.



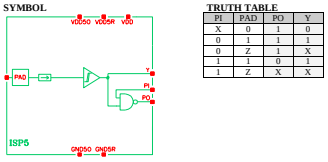
(a) APR00DF5 ([27] p.335)



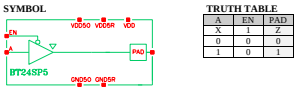
(b) VDDALLPADF5 ([27] p.350)



(c) GNDALLPADF5 ([27] p.345)



(d) ILP5 ([27] p.293)



(e) BT1P5 ([27] p.306)

Figure 43: *All the different pads used in the design*

Functions	Amount
VDDALLPADP5	
GND	12
GNDALLPADP5	
VDD	4
APR00DP5	
Digital Mux Output	1
Analog Mux Output	1
Inductor In	6
Inductor Out	6
DC/DC Out 1	3
Enable	1
LED	1
Feedback pin	1
BT1P5	
SPI MISO	1
ILP5	
SPI MOSI	1
SPI CLK	1
SPI SS	1

Table 12: *Specification*

4.2.4 | FSM

An overview of the FSM can be seen in Figure 44. It is connected to three other blocks: the oscillator, the master (SPI) and the analog design. For the SPI interface an existing

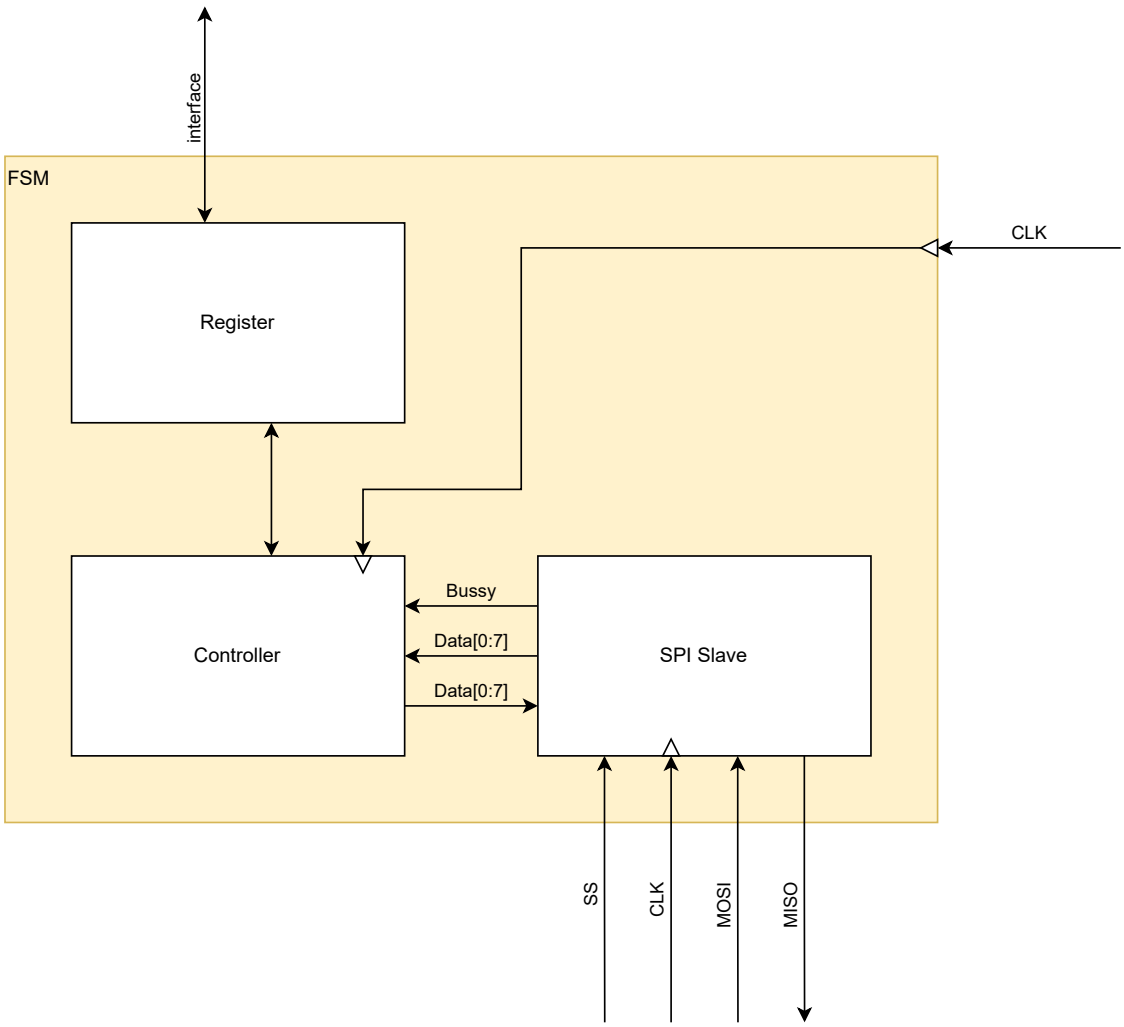


Figure 44: *Oscillator*

SPI slave module was used, which can also be seen in listening 2 [28]. For the controller it was decided to have a separate clock although it would be possible to use the SPI CLK only. The controller logic was implemented as a moore finite state machine as it can be seen in Figure 45.

To check if the syntheses was correct the amount of flip-flops expected was compared to the amount of flip-flops implemented in the design. The controller was implemented with eight registers from which six are read and write capable and two are read only. Furthermore the previous SPI command is always stored in register zero. Therefore one has in the end 7 registers that can be used to store data $\Rightarrow$ one expects that the hardware requires $\underbrace{8 \cdot 8}_{\text{registers}} + \underbrace{2}_{\text{finite state machine states}} = 58$ flip-flops for the finite state machine (the controller and its registers). The SPI block itself has two register (data to send and

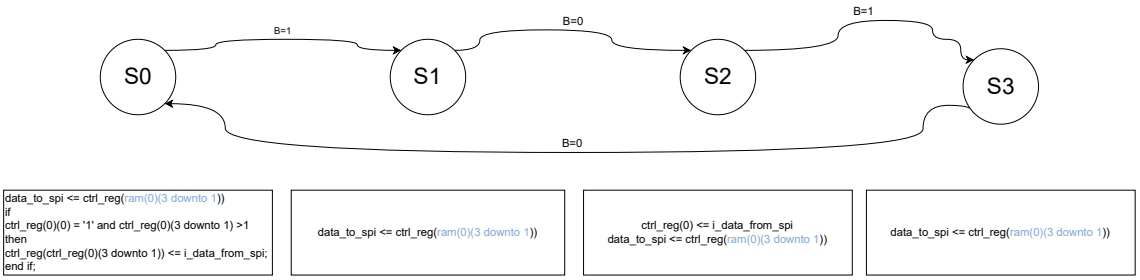


Figure 45: *FSM states*

data received) + the busy flag and therefore $\underbrace{8}_{\text{data to send}} + \underbrace{8}_{\text{data received}} + \underbrace{1}_{\text{busy flag}} = 17$ flip flops.
So total number of flip-flops is 73 which is also what one sees in the synthesis tool.

4.2.4.1 | Register Description

Register zero which can be seen in Figure 46 contains the current command.

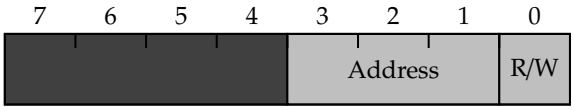


Figure 46: *r0*

Register one which can be seen in Figure 47 contains the status registers. Whereby one must say that in the current implementation non of those are implemented on the analogue side an therefore not used. But for a extended project they could be used.

- T_F: Over temperature.
- BB_{F_1}: Buck boost fault one
- BB_{F_1}: Buck boost fault two

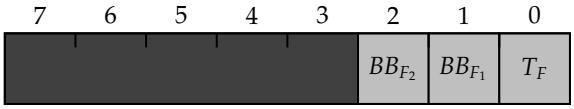


Figure 47: *r1*

Register two which can be seen in Figure 48 contains the analogue mux configurations. It allows to bring different internal analogue signals to the output. Thereby it is worthwhile to mention that only one analogue pin at the time can be put to the output, so it is not possible by wrong configuration to make a shortcut on the chip. The eight bits in this register can mux up to 256 different signal to the output, but the analogue design only uses ten different signals, as it can be seen in Figure 54

- AM_1:
- AM_2:
- AM_3:
- AM_4:

Register three which can be seen in Figure 49 contains the digital mux configurations, whereby one must say that with the current implementable one can only say if one wants

7	6	5	4	3	2	1	0
AM_7	AM_6	AM_5	AM_4	AM_3	AM_2	AM_1	AM_0

Figure 48: *r2*

7	6	5	4	3	2	1	0
DM_7	DM_6	DM_5	DM_4	DM_3	DM_2	DM_1	DM_0

Figure 49: *r3*

to output the clock or not.

- DM_1:
- DM_2:
- DM_3:
- DM_4:

Register six contains the tuning parameters of the oscillator capacitors. An example for writing and reading a register can be found in Figure 51 and Figure 50.

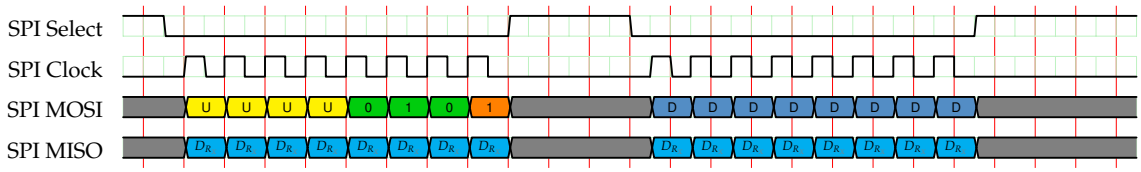


Figure 50: *Write example*

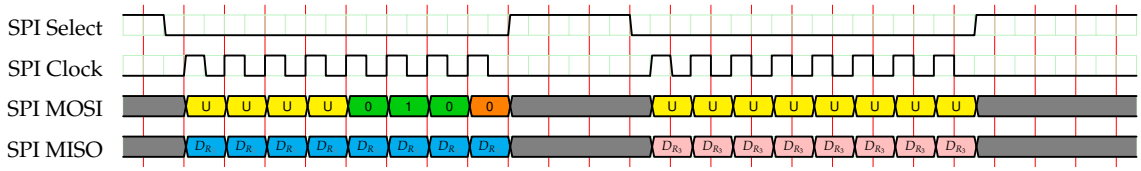


Figure 51: *Read example*

4.2.4.2 | Top Testbench

To verify the functionality of the ASIC in mixed signal mode, a comprehensive test bench was created, encompassing all blocks except the DC/DC converter. The test bench is illustrated in Figure 52, Figure 53, and Figure 54. During the test, a SPI sequence was generated to configure the analog testpin output of the ASIC. The goal of this emulation of the configuration process was to make the test as similar as with the physical ASIC in front of oneself. Since in the end one can also only measure the signals on the analog testpin. Additionally, it was examined what happens when the reset signal of the ASIC was pressed. The results of the test demonstrated that the ASIC operates as expected, allowing the multiplexing of different analog test signals to the output for measurement purposes.

To evaluate the functionality of the digital part of the circuit only, an additional test

bench was implemented using Vivado only. A screenshot of the test bench results can be observed in Figure 55. It is evident from Figure 55 that the SPI generator attempted to write the value 0xAA to register one, which is invalid since register one is designated as read-only as it can be read in subsubsection 4.2.4. So as expected in this case register one remained unwritten.
Subsequently, the content of register two was modified, as depicted in Figure 56 and Figure 57, yielding the expected results. The content of register two determines the multiplexing of a corresponding analog signal to the output and is therefore very important to have a testable chip.

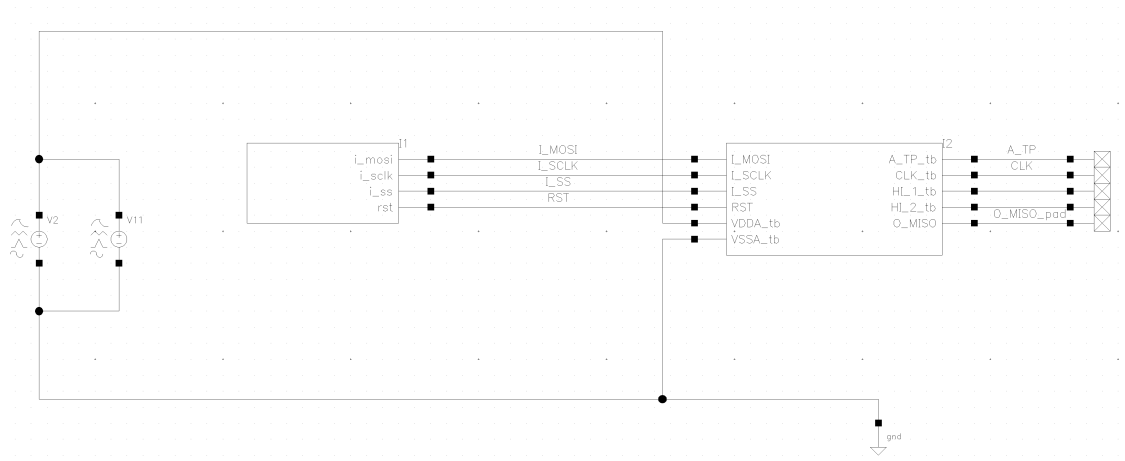


Figure 52: *Top test bench schematic, on the left the signal generator and on the right the ASIC*

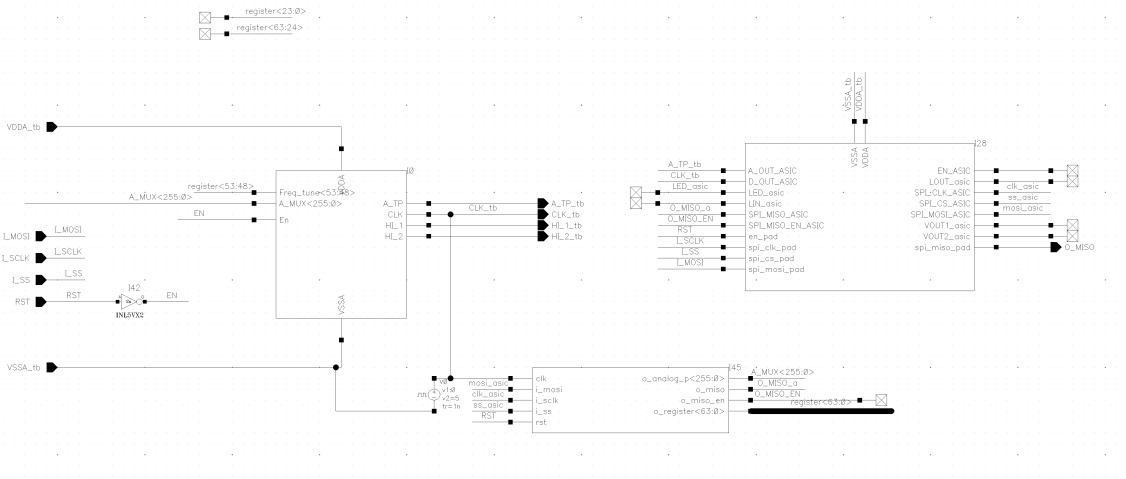


Figure 53: *ASIC top design with analog block, digital block and pad ring*

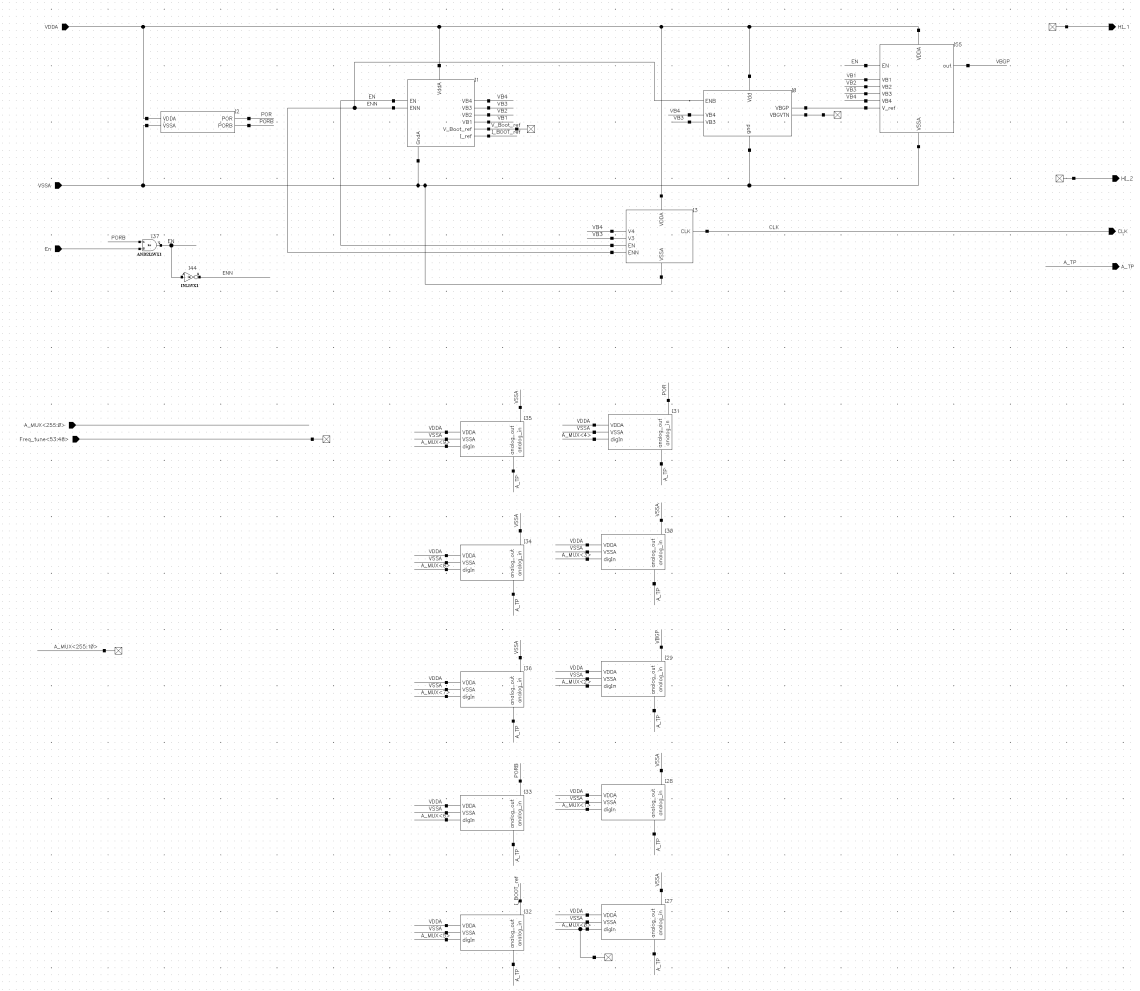


Figure 54: *Analog top with POR, Current reference, bandgap, linear regulator (to make sure bandgap signal has low impedance), transmission gates and oscillator, but without DC/DC converter*

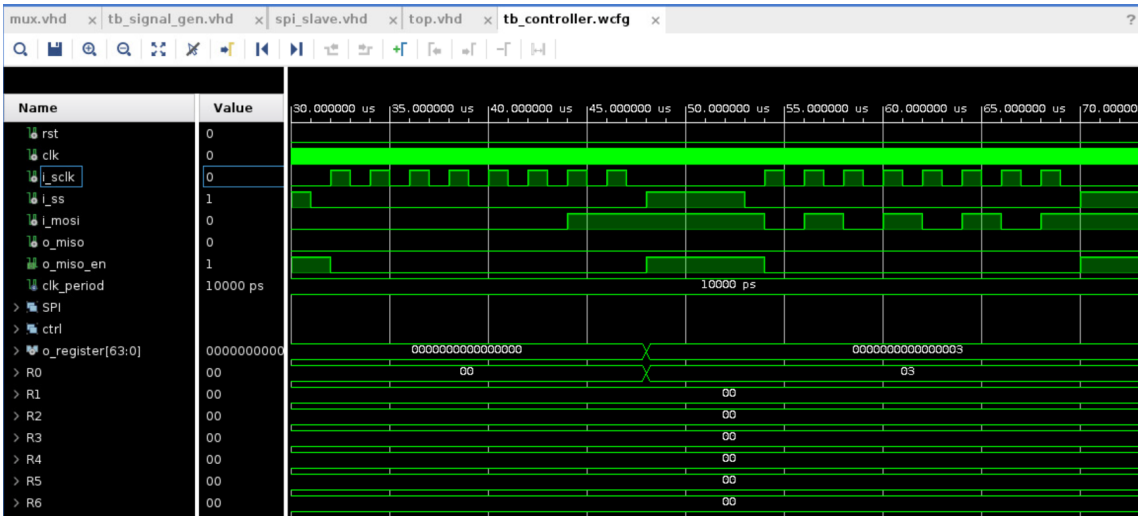


Figure 55: *SPI sequence that tries to write 0xAA to register one which is not possible as the screenshot shows.*

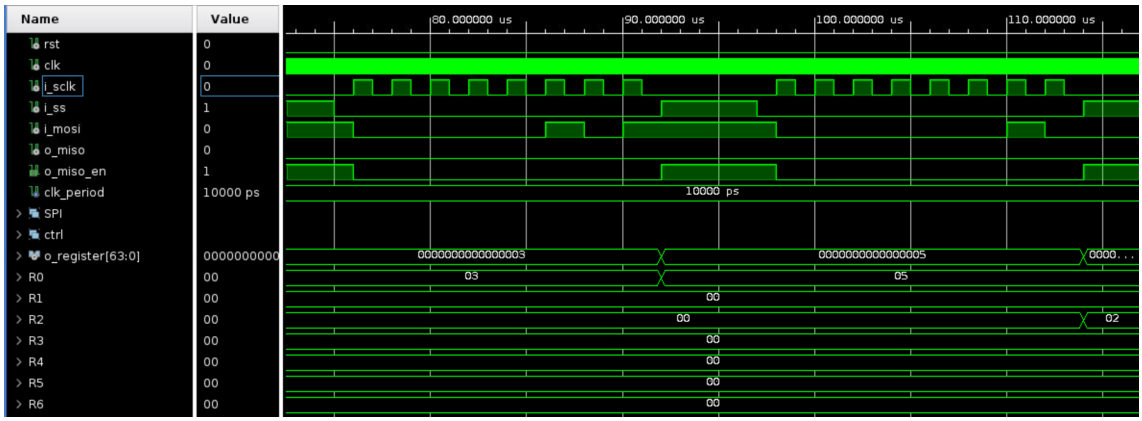


Figure 56: *SPI sequence that tries to write 0x02 to register two which is possible as the screenshot shows (R2 has value 0x02 in the end).*

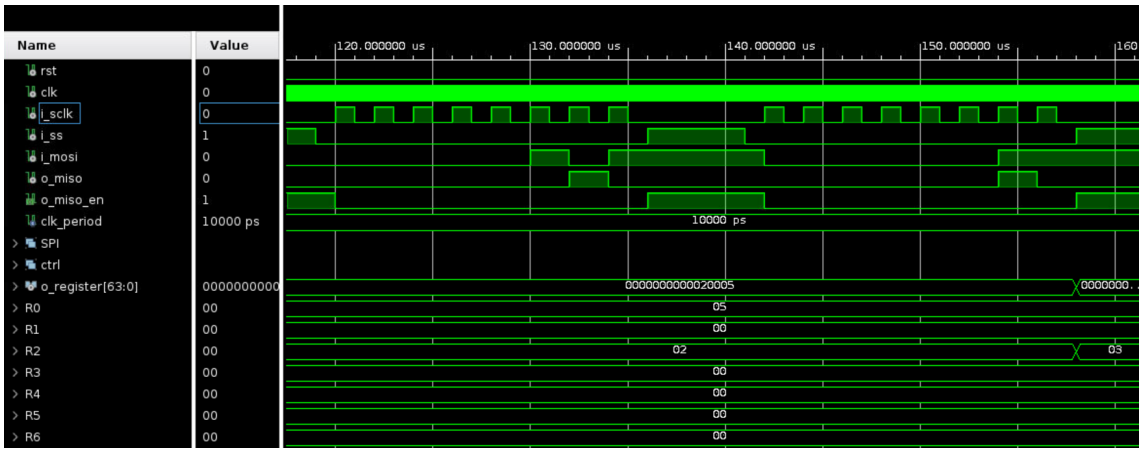


Figure 57: *SPI sequence that tries to write 0x03 to register two after it was already initialized to 0x02 which is possible as the screenshot shows (R2 has value 0x03 in the end).*

4.2.5 | Operational Transconductance Amplifiers (OTA)

As part of this design we required several OTAs. In total we designed four different designs, one with a NMOS royal differential pair, one with a PMOS royal differential pair and each with a variant with a reduced g_m. The OTAs with PMOS inputs are used in applications, where we need to amplify voltages close to GND. Those with NMOS inputs are used for applications, where the common-mode voltage is close to VDDA. The reduced g_m variants are needed in the control loop, in order to reduce the size of the compensation network (without the reduced g_m, the capacitors would not be manufacturable). A low g_m OTA with NMOS inputs is also used to amplify the voltage drop over the input power PMOS in the current sensing circuit. In this case, we take advantage of the linearization of the input transistor pair of the low g_m OTA. All OTAs we designed are simple folded cascode based circuits and are therefore very similar to each other. As such we will only present the figures for the low g_m OTA with PMOS inputs.

Characteristic	Nominal Value
GBP	2.2 MHz
Phase Margin	83°
Open Loop Gain	70.9 dB
Transconductance	14 µS
Output Resistance	250 MΩ
Input Offset Voltage (3σ)	21.1 mV
Quiescent Current	41.8 µA

Table 13: *Key specifications of the low g_m OTA with PMOS inputs and a* 1 pF *load*

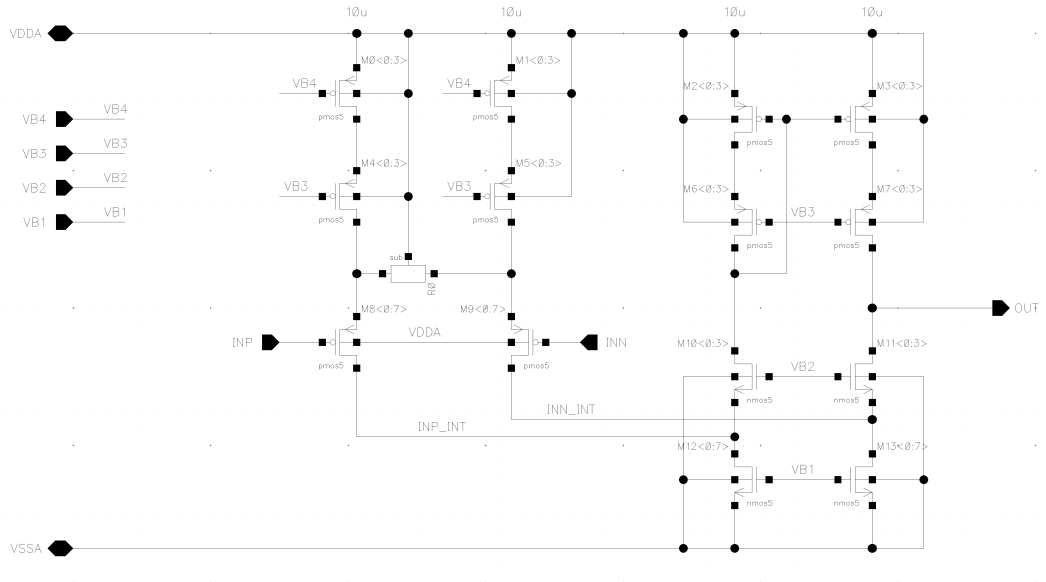


Figure 58: *Our implementation of a folded cascode OTA with PMOS inputs and a reduced g_m*

4.2.6 | Comparator

A comparator was originally to be used as the modulator in an average current-mode control scheme and we based our requirements on that application. The comparators in the A_CELLs library are not usable in this application, as they are optimized for low current consumption and not high speeds. They have propagation delay of around 500 ns, which is unacceptable for a switching frequency of 1 MHz. We therefore set out on making our own. The design we implemented is based on the circuit in Hans Camenzinds „Designing Analog Chips“, which itself is a fairly typical simple comparator circuit. Additionally we added a second output to make it have a differential output and increased the reference current of the circuit, until the comparator had a propagation delay of around 50 ns. The key specifications of the comparator we design can found in Table 14.

Characteristic	Nominal Value
Propagation Delay	51 ns
Rise Time(10% to 90%)	8.5 ns
Hysteresis	19.5 mV
Quiescent Current	27 µA

Table 14: *Key specifications of the comparator*

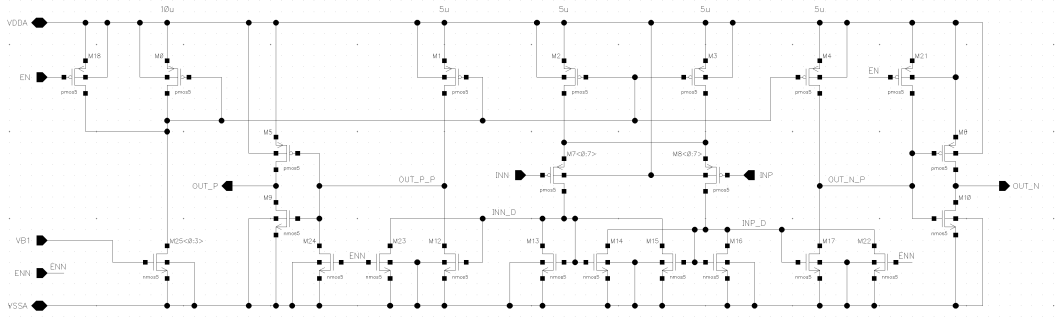


Figure 59: *Our implementation of a differential output comparator*

4.2.7 | SR Latch with Blanking Time

For the latch the blanking time we created our own out of basic CMOS components from the D_CELLS_L5V library. From the current sensing circuit we got the requirement for a 120 ns blanking time. We started by creating a simple SR latch out of two NOR logic gates. Instead of connecting the reset directly to the reset input, we added a AND gate to disable it. By using a discrete SR latch and a time delay circuit we are able to disable the reset input for a fixed amount of time, after the rising edge of the set input, thus creating a blanking time. For the delay elements we used 8 ns delay elements from the library and added extra capacitance to the output to further slow down the circuit. The blanking time directly effects the minimum PWM pulse-width, we therefore aimed to have the blanking time as short as possible, while still being longer than the minimum time required by the current measurement. The blanking time over our process corners can be found in

Table 15.

Characteristic	Value
Min. Blanking Time	117 ns
Typ. Blanking Time	145 ns
Max. Blanking Time	189 ns

Table 15: *Blanking time of the SR latch over the process corners*

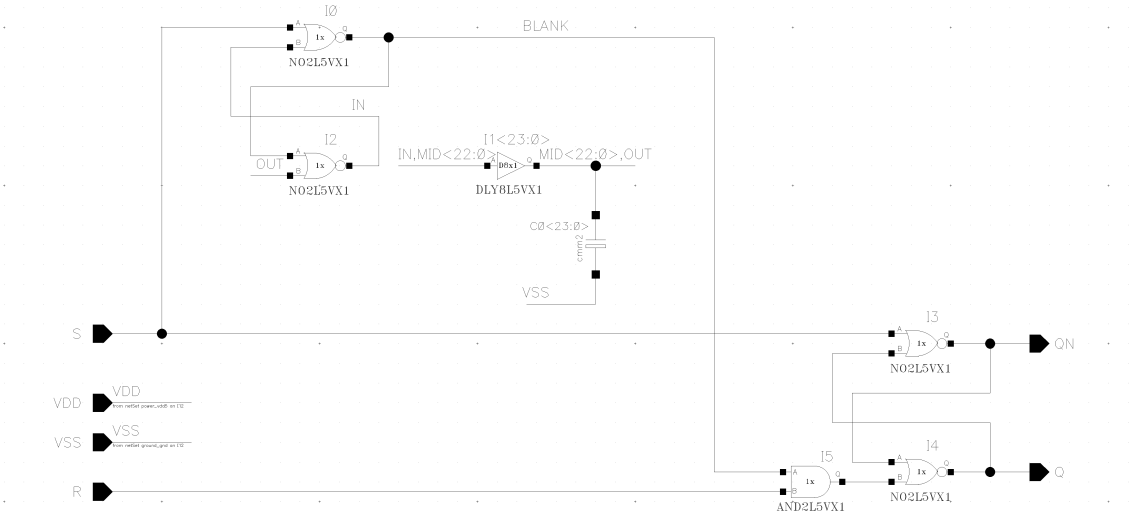


Figure 60: *Our implementation of a SR latch with blanking time*

4.2.8 | Current Measurement

For the current measurement we designed two different approaches. We will introduce both approaches as it took an extensive amount of time and it gave us a lot of insight into the advantages and disadvantages of both approaches. Firstly we will look at SenseFET based current measuring approach we implemented first, before switching to $R_{DS,on}$ current sensing.

In order to measure the current flowing through the inductor, we first implemented a SenseFET based current sensing circuit based on the proposed circuit in [29]. This circuit features some clever ideas like mirroring the measured current from the NMOS transistor into the PMOS SenseFET, in order for the upper control loop to already be in the correct operating region, when the switching transistors. As the circuit is already in the correct operating region, the loop requires less time to start tracking the current accurately. Using this approach the circuit tracks the inductor current accurately after a round 100 ns. This circuit unfortunately is not able to measure a reverse current flow, as in such a case, the COM voltage would be outside of the supply rails. We found no simple way to modify the circuit to allow for the measuring of the reverse current, we therefor had to abandon this approach.

After implementing the SenseFET based current measuring approach, we changed the regulator type to peak current-mode control, which lessened the requirements for the current measurement. We no longer had to measure the entire waveform, as we only

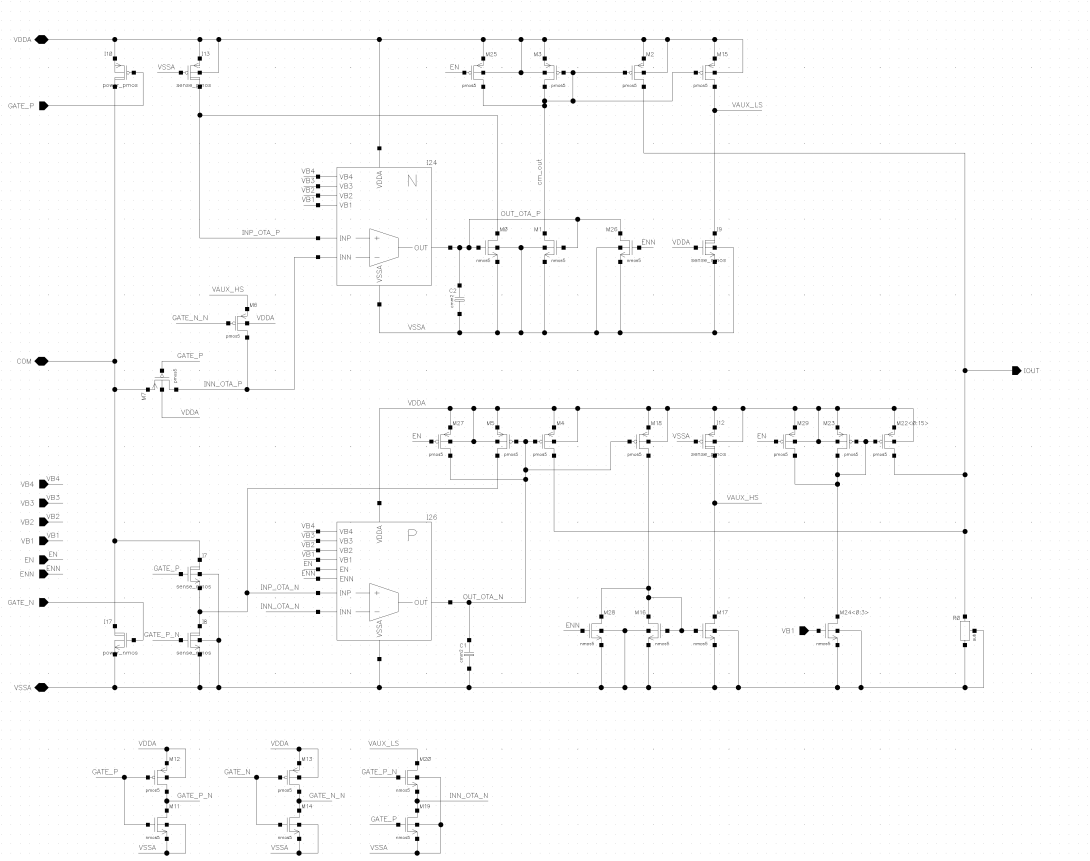


Figure 61: *Our implementation of a senseFET based full wave current sensing circuit*

need to know the peak current. This allows us to only measure the current flow during the rising period. By sensing and amplifying the voltage drop over the input PMOS, we can measure the rising edge of the inductor current. Using the $R_{DS,on}$ the input PMOS as a current shunt simplifies the design and also allows for the measurement of reverse current flow. For the amplifier we are using the low g_m NMOS input OTA we previously designed. As the input is linearized, the OTA has fairly constant g_m for small differential voltage applied to the input. We achieved a g_m of around 11 µS over the expected differential input range of $-10\,\text{mV}$ to $60\,\text{mV}$. These values correspond to a current flow of about $-100\,\text{mA}$ to $600\,\text{mA}$ in the switch, which is the range we expect to be operating in. In order to measure reverse current flow, we had to add an offset current to the output for the OTA to sink in such a case. The main characteristics of this circuit are listed in Table 16.

Characteristic	Value
Tracking Delay	120 ns
Transresistance	$2\,\text{V/A}$
Output Offset Voltage	580 mV

Table 16: *Characteristics of the $R_{DS,on}$ based current sensing circuit using a nominal* $180\,\text{k}\Omega$ *resistor to convert the output current into a voltage, as need by subsequent circuits*

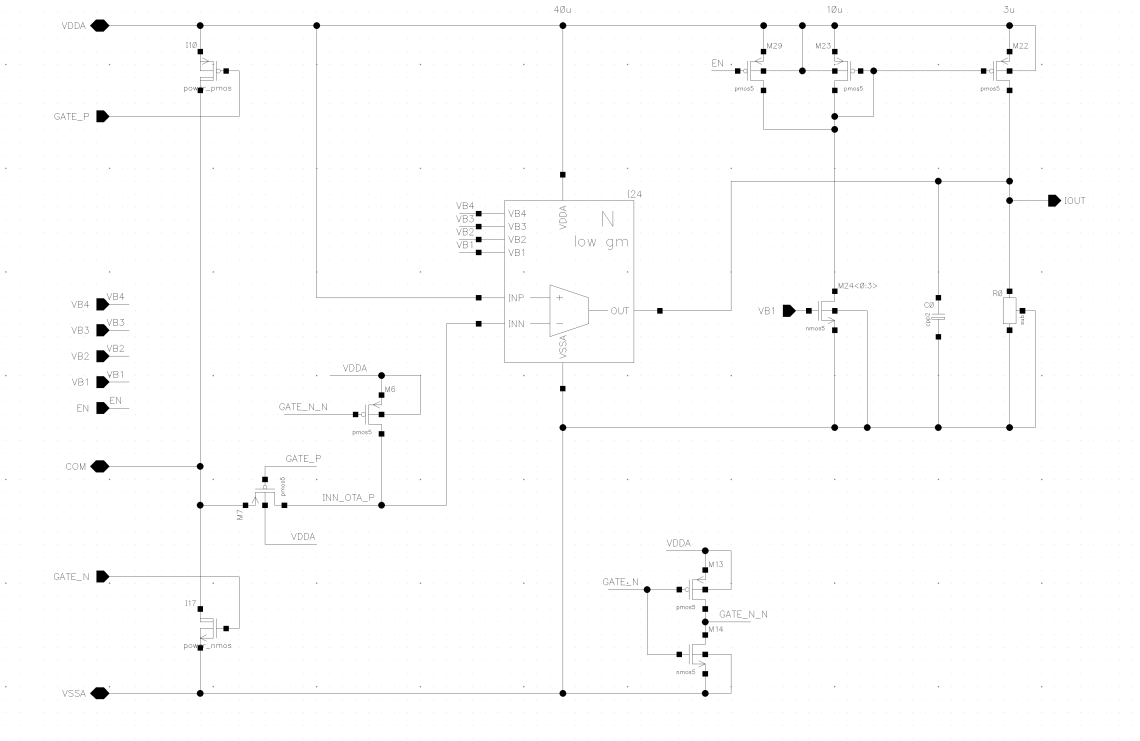


Figure 62: *Our implementation of a $R_{DS,on}$ based current sensing circuit*

4.2.9 | Timing and Slope Compensation

The DC/DC converter requires a 1 MHz clock to set the SR latch in the peak current-mode control loop and to generate the slope compensation required to make the loop stable. For the clock generator, we used the basic principle of charging a capacitor with a constant current and discharging it, as soon a it reaches a threshold voltage. The threshold was set to 2.4 V, as the circuit has to work with an input voltage as low as 4.3 V. Charging the capacitor like this creates a sawtooth voltage at the positive node of the capacitor and the discharge signal can be used as a pulse generator. For the slope compensation we want to create a sawtooth signal, which we can add to the value from the current measurement. As an addition of voltages is more difficult than the addition of two currents, we decided to have both outputs be current outputs. Over the capacitor we already have a sawtooth voltage, but as previously discussed, we need a sawtooth current for the slope compensation. In [30] they propose using two NMOS transistors to mirror the voltage from the capacitor onto a resistor, thus creating sawtooth current. This current can be modified by changing the value of the resistor. By mirroring the resistor to an output, we can create our slope compensation output current. Now we can connect the current output from the inductor current measurement, the current from thr slope compensation and a resistor to ground, in order to create a voltage representing the slope compensated inductor current.

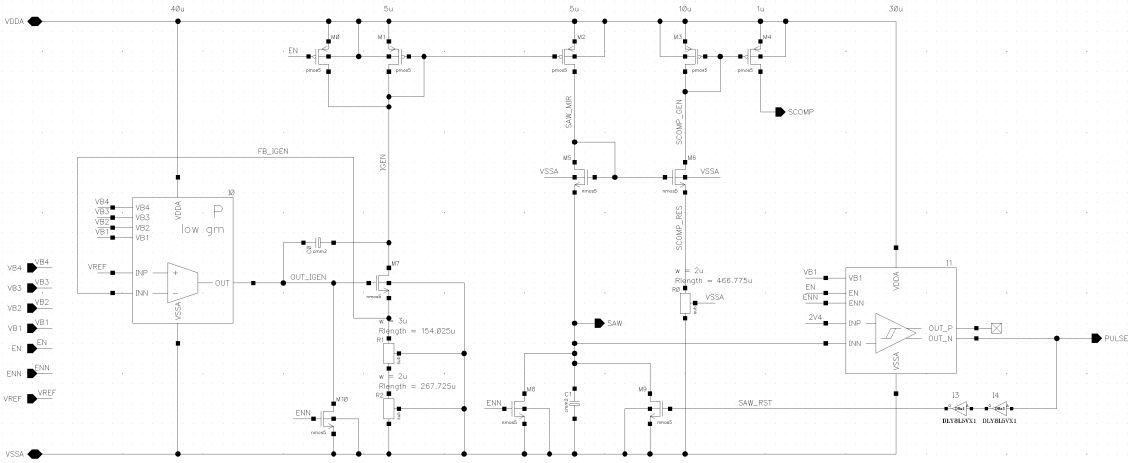


Figure 63: *Our implementation of a clock generator with a slope compensation output*

4.2.10 | Power MOSFETs

In order to switch the large inductor currents of over 400 mA, the switching transistors need to be sized accordingly. Our goal was to design switching transistors with a on resistance $R_{DS,on}$ of around 100 mΩ. It was however important, that the transistors have a good size and shape for the layout. We firstly designed small unit transistors, out of which we could later build a mosaic, in order to create the large switching devices. Each unit transistors contains two transistors and have the such that, when ordered in a mosaic, all transistors are automatically correctly connected to each other and no design rules are violated. To protect the transistors from the snapback effect, we extended the drain, as recommended in the XFAB documentation. This forced us to widened the gate of the transistors to 800 nm from 600 nm, to not violate any design rules. The lengthened gate increased the $R_{DS,on}$, but we were still able to reach out target of around 100 mΩ.

Characteristic	Value
Typ. $R_{DS,on}$	113 mΩ
# of Transistors	4834
Width	96.7 mm
Size	1000.2 µm x 486.8 µm

Table 17: *Specifications of the power PMOS*

Characteristic	Value
Typ. $R_{DS,on}$	72.8 mΩ
# of Transistors	2800
Width	56 mm
Size	641.4 µm x 483.1 µm

Table 18: *Specifications of the power NMOS*

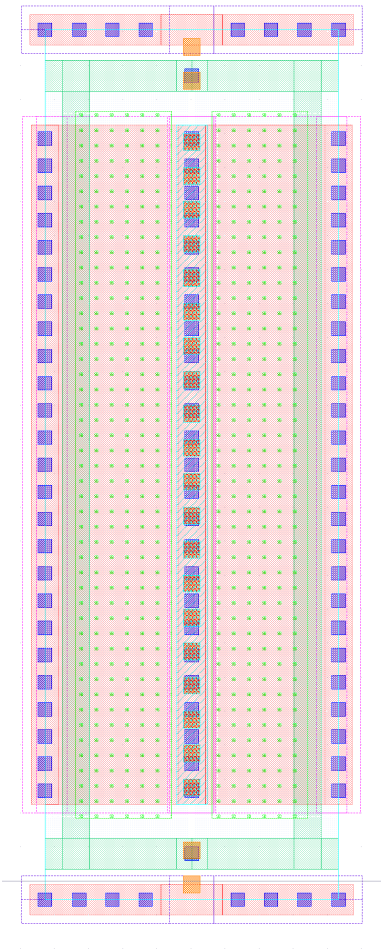


Figure 64: *The layout of our unit NMOS transistor containing two* 20 µm/800 nm *NMOS transistors with extended drains*

4.2.11 | Level Shifter

In order to correctly drive the output PMOS correctly, the have to drive its gate with the voltage at its source which is connected to the output node. As all internal supplies are directly connected to input node, we have to cross voltage domains to drive the output transistors, thus requiring a level shifter. Even though the level shifter is only needed of the output half-bridge, we want to only create one gate driver circuit for both half-bridges and are therefore using level shifters at the input of the each gate driver. As the output voltage can higher or lower than the input, the conventional level shifter from the XFAB libraries can not be used, as it requires the output voltage to always be higher than the input. A single supply level shifter solves this problem by only needing one supply connected to the output. We designed our level shifter based on the circuit described in [31], while sizing the transistor based on the default sizes and drive strengths of CMOS circuits in XFAB libraries.

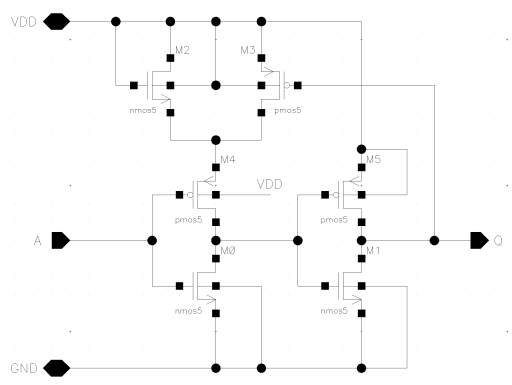


Figure 65: *Our implementation of a single supply level shifter*

4.2.12 | Non-overlapping Gate Driver

The function of the gate driver is to convert the low power output signal from the flip-flop to a high-current output capable of driving the the power MOSFETs. As the power MOSFETs have a significant size the have a significant gate capacitance which stores a significant gate charge. At every switching cycle the gate charge needs be completely added and removed. As this process takes time, it is important to ensure that both power MOSFETs are not conducting at the same time, as this would cause a large current flowing from the supply through the MOSFETs directly to ground in process called shoot-through. The prevent this we have to ensure the PMOS is competently turned off before turning on the NMOS and vice-versa. To do this we use a non-overlapping driver circuit, which introduces a fixed delay between both drive signals.
We have implemented the typical non-overlapping control circuit out of digital cells from XFAB library. In order to drive the large gates of the switching transistors, we used a series of inverters with increasing drive strength. The last stage uses one inverter with X4 drive strength to drive each gate strand of PMOS transistors and one inverter with X2 drive strength for the NMOS transistors. In addition we have an enable pin to turn off the both power MOSFETs to turn off all switching transistors, bringing them into a safe state. As it possible for the output voltage to be greater than the supply voltage of the chip, we need to translate the voltage levels from the drive signals to the supply level of the gate driver. For this we used the previously described single supply level shifters we designed.

4.2.13 | Thermal Shutdown

In order to protect circuits from sustained overload load conditions a thermal shutdown circuits is often employed. The goal is to measure the silicon temperature near the most heat generating parts of the chip and turn off the heat generating sub-circuits if the temperature exceeds a predefined limit. A crude temperature measurement often suffices. Thermal Shutdown (TSD) circuits also use hysteresis to prevent the circuit from rapidly shutting down and turning on again. We found the hysteresis of ICs on the market to be around 20 °C to 40 °C and have a trip point of 140 °C to 170 °C. We based our thermal shutdown circuit on the circuit found in the XFAB A_CELLS Library. As this circuit is

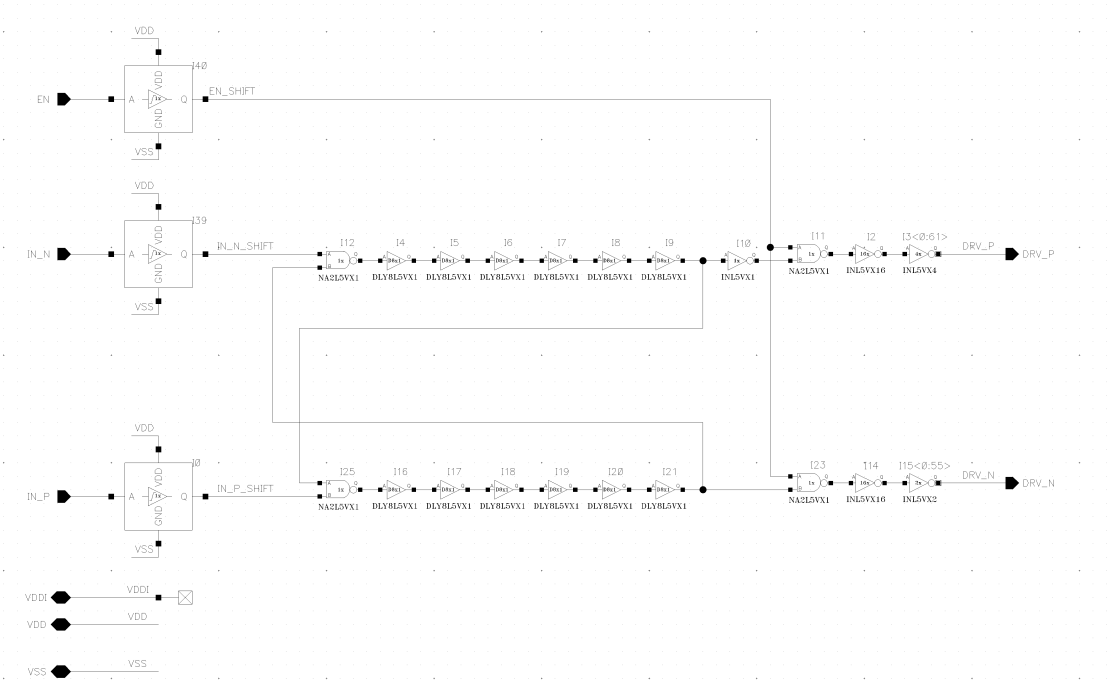


Figure 66: *Our implementation of a gate driver with non-overlapping drive signals*

not suitable for a 5 V supply and requires their complementary circuitry to work, we modified it to work in our design. Firstly we changed all MOSFETs to their 5 V variants, used or own folded cascode to generate a reference current in the circuit and used the comparator we already designed. In addition we added M9 to the circuit to increase the current in one strand in the case of an over temperature event to increase the hysteresis of the circuit. Without it the hysteresis is only 7 °C and we wanted to increase it to around 30 °C to be more in line with the values seen in other designs.

The circuit works by comparing the forward voltage of two strands of bipolar transistors wired in a diode configuration. The two stands are designed such that both have similar forward voltages at room temperature, but different temperature coefficients. The strands with higher temperature coefficient starts hat a higher voltage at room temperature, but at some higher temperature falls bellow the voltage created by the other strand. This crossover is detected with a comparator, and we will call the temperature at with this crossover happens the crossover temperature. The different temperature coefficients are achieved by using one strand with three series diodes and another with four. By sending a significantly smaller current through the strand with four transistors, the forward voltages are set to level slightly higher then the one in the other strand. As the strand with four transistors has more transistors in series, its forward voltage has larger temperature dependence. By varying the the current through both strands it possible to relatively precisely set the crossover temperature of the circuit. As the voltage of both strands is generated by using the forward voltage of bipolar transistors, both are subjected to the same process variations with can be seen in the very stable crossover temperature over the process corners. We have set the currents such that we get a crossover temperature of

140 °C and a hysteresis of 30 °C.

Device	Trip point	Hysteresis
Texas Instruments TPS63000	140 °C	20 °C
Renesas ISL9122A	130 °C	25 °C
Maxim MAX8625A	165 °C	15 °C
ST Microelectronics STBB2	150 °C	20 °C
This Design	140 °C	30 °C

Table 19: *Overview of thermal shutdown settings of various buck-boost converters*

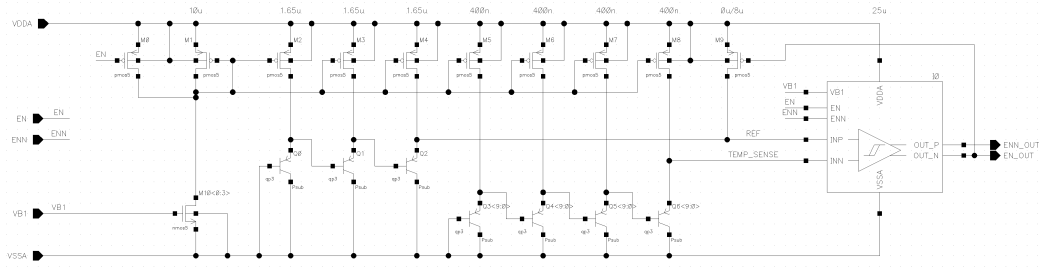


Figure 67: *Our implementation of an over-temperature protection circuit*

5 Specifications

Description	Explanation	min	avg	max	Unit	Comment
DC/DC						
Turn Off Time	When unplugged the output voltage must decrease to less than two volts within 10s.			10	s	
Input Voltage	Charger is operating in this range	4.3		5.5	V	
Converter Type	Buck boost converter					
Max Input Voltage	Charger get not damaged with this voltage	5.5			V	
Max Charging Current		200			mA	
Average Output Voltage		4.9		5.1	V	
Output Voltage Ripple	Peak Peak			50	mV	
Efficiency	at 200mA	80%			V	
Interface						
SPI	Must support SPI					
Registers	Can write configuration registers					
USB-C	compatible with USB-C					
Safety						
Temperature Range	[32]	0		70	°C	
Mechanical						
Size	From MPW			10	mm^2	

Table 20: *Specification*

6 Results

In this chapter we will present main result as we have simulated so far. As the layout is not yet finished, all results presented here done pre post-layout-simulation and are subject to change. The focus of the results here are in relation to the performance of the buck-boost converter. While all sub-circuits were simulated over all expected process corners and some where necessary with Monte-Carlo simulations, the system level simulations presented here only done under nominal circumstances due to time constraints. We have identified three key areas of interest that we will discuss further. The first is regarding the start up behavior of the circuit. The converter should be able to start and regulate the output voltage and current sufficiently, without a significant load present as well as under maximum specified out. The next area of interest is regarding the dynamic regulation characteristics. Here we are applying a step to the input voltage and conducting a load step to the output. Lastly we want to test the behavior of the converter, when a short circuit to ground is applied to the output. In all following waveforms the output voltage is yellow and the inductor current is in red.

6.1 Startup Behaviour

The first test shows the circuit starting up without a load present. For this test we apply the nominal 5 V to the input and enable the converter, while pulling only 1 mA from the output. The current limiting works as expected, limiting the current to roughly 550 mA while starting. The output voltage overshoots the 5 V target by about 230 mV. While this is more then we previously expected, this is not surprising, as all the energy stored in the inductor gets dumped into the output capacitor.

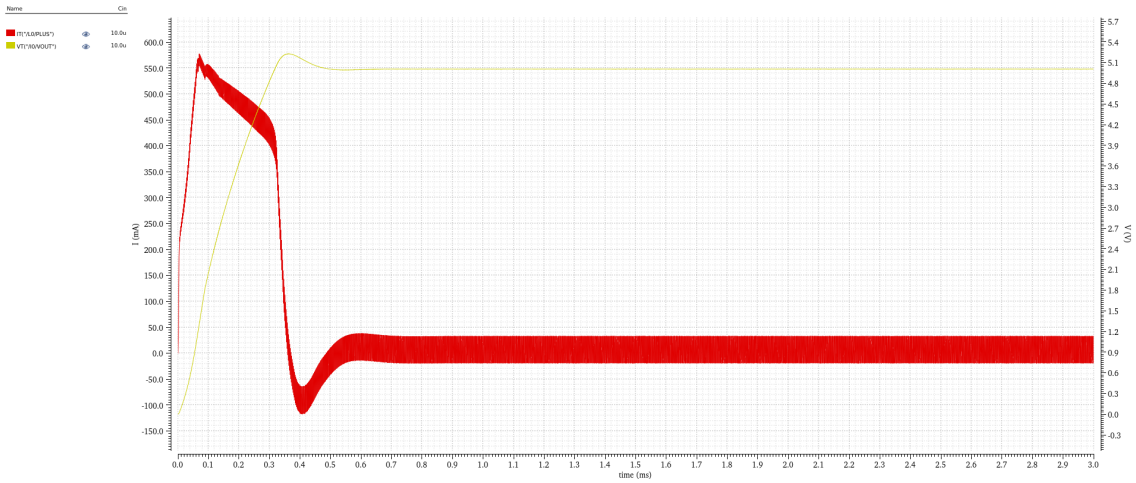


Figure 68: *Results of starting up the converter with a* 1 mA *load*

Characteristic	Value
Overshoot	230 mV
Average Voltage	5.009 V
Output Ripple	5.8 mV

Table 21: *Results of starting up the converter with a* 1 mA *load*

The results from starting the converter with a 200 mA load are more pleasing. The output voltage overshoot is significantly less at 49 mV. In Figure 69 it is possible to see the foldback current limit working. For low output voltages under 1.2 V the current is proportionally limited in accordance with the output voltage. After reaching the output voltage threshold, the current is, more or less, limited to a constant value before the regulator starts taking over. In both startup cases the average output voltage as well as the output voltage ripple are at satisfactory levels. The efficiency of the converter under full load is 91.6 %.

Figure 69: *Results of starting up the converter with a* 200 mA *load*

Characteristic	Value
Overshoot	49 mV
Average Voltage	5.049 V
Output Ripple	10.2 mV
Conversion Efficiency	91.6 %

Table 22: *Results of starting up the converter with a* 200 mA *load*

6.2 Dynamic Regulation Behavior

The following two test can be categorized as dynamic regulation behavior. In both cases the regulator is allowed to reach steady-steady before applying a violent change at the input or output respectively. In the first case we step the input voltage from 4.3 V to 5.5 V and back, e.g from the minimum value specified value to the maximum. In the second case will step the load current from 1 mA to 200 mA and back, again from the minimum value specified value to the maximum. Our goal is to examine the effects on the output

voltage and current regulation. The input voltage step only leads to a small disturbance to the output voltage and is quickly eliminated.

Figure 70: *Results of applying a input voltage step of* 4.3 V → 5.5 V → 4.3 V

Characteristic	Value
Overshoot	34.8 mV
Droop	20 mV

Table 23: *Results of applying a input voltage step of* 4.3 V → 5.5 V → 4.3 V

Applying the load step causes a more severe disturbance to the output, which is to be expected. The output voltage droops around 175 mV bellow its target, when the load is applied and overshoots the target by 185 mV when the load is removed. Nonetheless the disturbance is corrected in less than 200 µs.

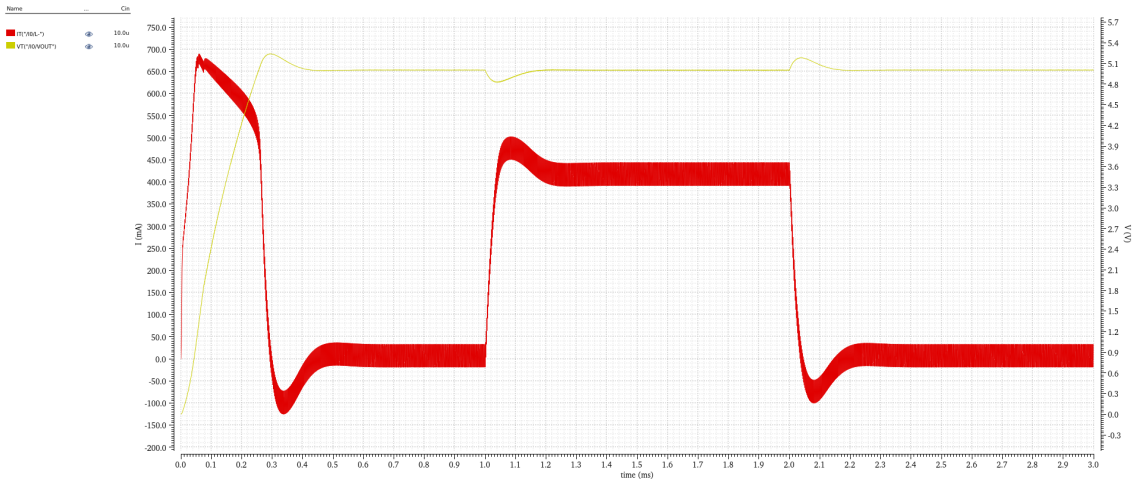


Figure 71: *Results of applying a load step of* 1 mA → 200 mA → 1 mA

Characteristic	Value
Overshoot	185 mV
Droop	175 mV

Table 24: *Results of applying a load step of* 1 mA → 200 mA → 1 mA

6.3 Current Limiting

In order to test the current limiting behavior of the circuit, we simulated the startup behavior of the circuit with the output short circuited to ground. The simulated waveforms can be seen in Figure 72 and shows the current being limited to 286 mA. This value is lower then the general current limit of 550 mA, showing the circuit operating as intended and keep the component stresses low in the case of a shorted output.

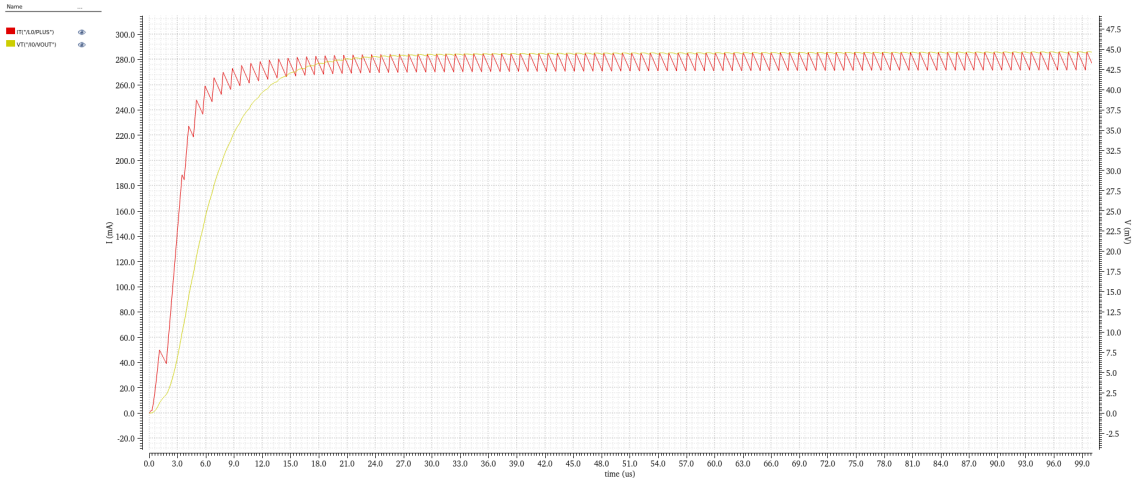


Figure 72: *Results of starting up the converter with a shorted output*

Characteristic	Value
Max. Inductor Current	286 mA

Table 25: *Results of starting up the converter with a shorted output*

7 | Conclusion

We were able to achieve our goal of designing a highly integrated buck-boost converter IC, which meets the specifications given to us by the Sonova AG. The peak-current control based converter is able to accurately create a output voltage both higher and lower than its input. The output voltage can be maintained over the whole specified input voltage range and regulator can quickly react to changes on the input and output. To ensure save operation the design features a foldback over-current protection, which leads to a short circuit safe output and basic soft-start functionality. To protect the switching transistor from over-temperature induced failure, we implemented thermal shutdown mechanism, which safely shuts off the converter if the transistors get to hot. We were not able to meet the deadline for the the tape-out, as we had to change the converter topology late in the process and due to the significant time required in the layout stage of the design.

We faced a steep learning curve as both of us were unfamiliar we the tools as we started the project. Consequently, our initial timeline was to optimistic and had to be adjusted as the design and layout efforts required more time than anticipated. We sincerely appreciate the opportunity given to us by the university and department IMES to work on such an ASIC project. However, we acknowledge the scope of the project was overly ambitious for a master's project, resulting in a significant higher time investment than anticipated. Therefore, we recommend to our supervisor and expert that future projects should be smaller in scale, particularly if the participants are not proficient users of the design tools required, as a substantial amount of time was dedicated to learning the program and troubleshooting errors, rather than focusing on design aspects.

Having completed the pre-layout phase, we have successfully defined all the parameters necessary for measuring the ASIC. The system design simulation has indicated that the ASIC should function as intended, giving us confidence that the final ASIC will work accordingly and we can proceed as planned.

8 Outlook

8.1 Time-plan

Since the pre-layout phase is finished with this document. The next important phase is the layout phase and then the tape-out. According to our actual plan which can also be found online under the following link[5] the tape out is planned in October 2023. So that we get the first physical ASIC's somewhere in April. During the time period where we wait on the ASIC's we will already prepare the test script and adapter PCBs to test all the specified parameters on the chip.

8.2 Hours

Jira, which allows time tracking, was utilized by one project participant to monitor the hours dedicated to specific tasks. This feature provides a high-level overview, as shown in Figure 73, depicting the distribution of hours across different project segments, referred to as epics in Jira. It is important to note that this data reflects the input from only one participant, as the other participant ceased reporting his hours. Notably, a significant portion of time was invested in system design. However, it is worth mentioning that this category encompasses time spent on debugging and configuring Cadence for accurate simulations. Additionally, 108 hours have been allocated to layout work, although only a few blocks have been completed thus far. Considering future planning, it is evident that the period leading up to tapeout will be demanding, leaving no room for additional implementations on the ASIC before tape-out.

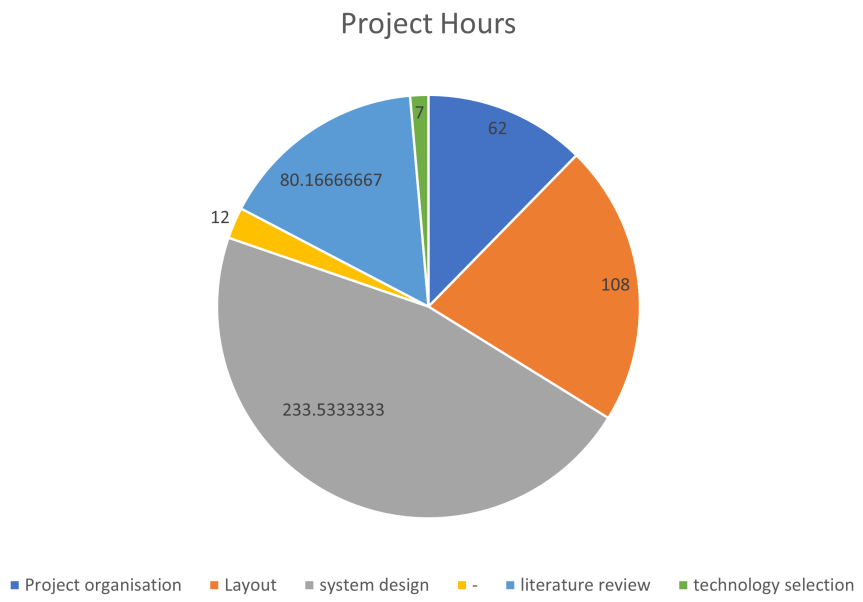


Figure 73: *Project hours and distribution of one participant only so far (05.07.2023)*

[5] https://asic-project.atlassian.net/jira/software/projects/MAP/boards/3/timeline

9 | Declaration of Authorship

Declaration

We hereby declare that we have independently completed the present work without any assistance from third parties that were not mentioned in this document. We have only used the resources and tools that we have specified. Thoughts and ideas taken from external sources, whether directly or indirectly, have been appropriately acknowledged. The work has not been submitted to any other examination authority or previously published.

Place	**Date**
Rapperswil	July 14, 2023

Signature Matthias Meyer Patrick Jansky

10 | Listings

List of Abbreviations

ASIC Application Specific Integrated Circuit

BJT Bipolar Junction Transistor

CCM Continous Conduction Mode

CMOS Complementary Metal–Oxide–Semiconductor

DCM Discontinous Conduction Mode

ESD Electrostatic Discharge

FET Field-Effect Transistor

FSM Finite-State Machine

GgNMOS Gate-Ground-NMOS

HI Hearing Instruments

IC Integrated Circuit

I2C Inter-Integrated Circuit

LDO Low Drop-Out

MOS Metal-Oxide Semiconductor

MOSFET Metal-Oxide Semiconductor Field-Effect Transistor

MPW Multi Project Waver

NMOS N-Type Metal-Oxide Semiconductor

OTA Operational Transconductance Amplifier

PFM Pulse-Frequency Modulation

PMOS P-type Metal-Oxide Semiconductor

POR Power-on-Reset

PWM Pulse-Width Modulation

SCR Silicon Controlled Rectifier

SEPIC Single-Ended Primary-Inductor Converter

SPI Serial Peripheral Interface

TSD Thermal Shutdown

UART Universal Asynchronous Receiver/Transmitter

USB Universal Serial Bus

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11 | Appendix

11.1 | Graphics

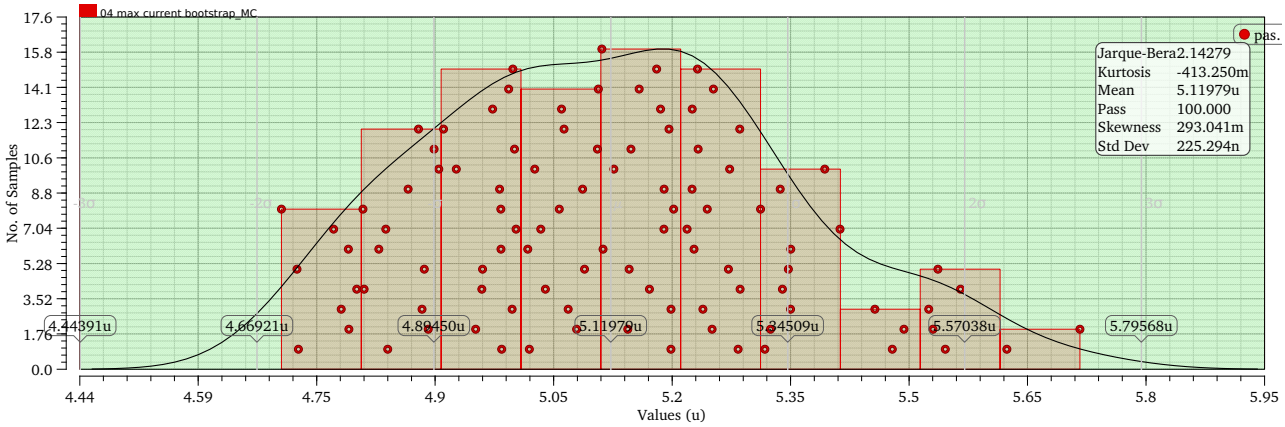

Figure 74: *Monte Carlo distribution of the first Current reference, which had a reference current of* 5 µA.

11.2 | Code

```vhdl
-- Created by Matthias Meyer
-- 16/12/2022

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
library work;
use work.ctrl_pkg.all;

entity ctrl is
--generic();           -- Data width of a register
Port (
    o_busy                      : in std_logic;                             -- spi is receiving data if '1' ==> i_data_from_spi is not stable
    --o_data_to_spi               : out  std_logic_vector(c_DW-1 downto 0);     -- register which is sent to spi
    --i_data_from_spi             : in std_logic_vector(c_DW-1 downto 0);       -- register received from spi
    o_data_to_spi               : out  std_logic_vector(7 downto 0);      -- register which is sent to spi
    i_data_from_spi             : in std_logic_vector(7 downto 0);        -- register received from spi
```

```
18      clk                         : in std_logic;                                 -- clk
        ↪  for module
19      rst                         : in std_logic;                                  --
        ↪  reset signal for module
20      --o_register                  : out std_logic_vector(2**c_AW*c_DW-1 downto 0)
        ↪  --output register
21      o_register                  : out std_logic_vector(63 downto 0)      --output
        ↪  register
22    );
23  end ctrl;
24
25  architecture rtl of ctrl is
26      type state is (S0, S1, S2, S3);
27      signal c_st, n_st : state;
28      --define ctrl_reg
29      signal ctrl_reg : t_register := ((others=> (others=>'0')));
30  begin
31      --
32      o_register <= to_slv(ctrl_reg);
33      -- memorizing process
34      p_seq: process (rst, clk)
35      begin
36          if rst = '1' then
37              c_st <= S0;
38  --            ctrl_reg <= (others=> (others=>'0'));
39          elsif rising_edge(clk) then
40              c_st <= n_st;
41          end if;
42      end process;
43      -- memoryless process
44      p_com: process (o_busy,i_data_from_spi, ctrl_reg, c_st, rst)
45      begin
46      -- default assignments
47      n_st <= c_st; -- remain in current state
48      --data to spi is value of the register with the address stored in register zero
49      o_data_to_spi <= ctrl_reg(to_integer(unsigned(ctrl_reg(0)(3 downto 1))));
50      -- specific assignments
51      case c_st is
52          when S0 =>
53              if o_busy = '1' then n_st <= S1;
54              end if;
55              --if write is set to one and register address is larger than one then
                ↪  write register.
```

```
56              if ctrl_reg(0)(0) = '1' and unsigned(ctrl_reg(0)(3 downto 1)) >
                ↪  to_unsigned(1,3) then
57                  ctrl_reg(to_integer(unsigned(ctrl_reg(0)(3 downto 1)))) <=
                    ↪  i_data_from_spi;
58              end if;
59          when S1 =>
60              if o_busy = '0' then
61                  n_st <= S2;
62              end if;
63          when S2 =>
64              if o_busy = '1' then n_st <= S3;
65              end if;
66              ctrl_reg(0) <= i_data_from_spi;
67          when S3 =>
68              if o_busy = '0' then n_st <= S0;
69              end if;
70          when others =>
71              n_st <= S0; -- handle parasitic states
72      end case;
73      end process;
74  end rtl;
75
76
77
```

Listing 1: ctrl

```
1
2   -- Source code from https://surf-vhdl.com/spi-slave-vhdl-design/
3   -- Modified by Matthias Meyer
4   -- 16/12/2022
5
6
7   library ieee;
8   use ieee.std_logic_1164.all;
9   use ieee.numeric_std.all;
10
11  entity spi_slave is
12  generic(
13    N                     : integer := 8;       -- number of bit to serialize
14    CPOL                  : std_logic := '0' );  -- clock polarity
15   port (
```

```
16    o_busy                    : out std_logic;  -- receiving data if '1'
17    i_data_parallel           : in  std_logic_vector(7 downto 0);  -- data to sent
18    o_data_parallel           : out std_logic_vector(7 downto 0);  -- received data
19    i_sclk                    : in  std_logic;
20    i_ss                      : in  std_logic;
21    i_mosi                    : in  std_logic;
22    o_miso                    : out std_logic);
23  end spi_slave;
24
25  architecture rtl of spi_slave is
26
27  signal r_shift_ena                          : std_logic;
28  signal r_tx_data                            : std_logic_vector(N-2 downto 0);  --
    ↪  data to sent
29  signal r_rx_data                            : std_logic_vector(N-1 downto 0);  --
    ↪  received data
30
31  begin
32  o_data_parallel  <= r_rx_data;
33  o_busy           <= r_shift_ena;
34
35  p_spi_slave_input : process(i_sclk)
36  begin
37    if(i_sclk'event and i_sclk=CPOL) then -- CPOL='0' => falling edge; CPOL='1' =>
      ↪  risinge edge
38      if(i_ss='0') then
39        r_rx_data             <= r_rx_data(N-2 downto 0)&i_mosi;
40      end if;
41    end if;
42  end process p_spi_slave_input;
43
44  p_spi_slave_output : process(i_sclk,i_ss)
45  begin
46    if(i_ss='1') then
47      r_shift_ena             <= '0';
48      o_miso                  <= 'Z';
49    elsif(i_sclk'event and i_sclk= not CPOL) then -- CPOL='0' => falling edge; CPOL='1'
      ↪  => risinge edge
50      r_shift_ena           <= '1';
51      if(r_shift_ena='0') then
52        o_miso                <= i_data_parallel(N-1);
53        r_tx_data             <= i_data_parallel(N-2 downto 0);
54    else
```

```
      o_miso                <= r_tx_data(N-2);
      r_tx_data             <= r_tx_data(N-3 downto 0)&'0';
    end if;
  end if;
end process p_spi_slave_output;

end rtl;
```

Listing 2: spi slave

```
clear
%pkg load control;
%% Controller Parameters
% RC Low Pass
Rf = 200e3;
phitp = 0.5; %phitp = fctp/fs

%Inner Current Controller
gmi = 13.56e-6;
R1i = 1/gmi;
%R1i = 1e3;
fci = 100e3; % Bandwidth %30k
PMi = 60;   % Phase margin

%Outer Voltage Controller
gmv = 13.56e-6;
R1v = 1/gmv;
%R1v = 1e3;
fcv = 10e3; % Bandwidth %10k
PMv = 72;   % Phase margin

%Current Sensor Voltage Offset
VOFF = 0.5;

%% Physical Parameters
Vi = 5;
Vo = -5;
L = 47e-6;
C = 22e-6;%120
fs = 500e3;
RL = 25;
rC = 0.01;
```

```
rL = 0.01;

D = 0.5;
%D = 0.3213;
IL = -Vo/(RL*(1-D));

r = 0.1;
% RF = 0.07;
% rDS = 0.11;
% r = D*rDS+(1-D)*RF+rL;

VTm = 3;
%Rs = 1;
VRV = 1.25;

%% Duty Cycle-to-Output Voltage Transfer Function Tp

Tp0 = -(Vo/(D*(1-D)))*(D*r-((1-D)^2)*RL)/(r+((1-D)^2)*RL); %%DC Gain
Tpx = (-Vo/(1-D))*(rC/(RL+rC));
omega0 = sqrt((r+((1-D)^2)*RL)/(L*C*(RL+rC)));
zeta = (L+C*(r*(RL+rC)+((1-D)^2)*RL*rC))/(2*sqrt(L*C*(RL+rC)*(r+((1-D)^2)*RL)));
omegazn = 1/(C*rC);
omegazp = (RL*((1-D)^2)-D*r)/(D*L);

fo = omega0/(2*pi);
fzn = omegazn/(2*pi);
fzp = omegazp/(2*pi);

Tp = Tpx*tf([1 omegazn-omegazp -omegazn*omegazp], [1 2*zeta*omega0 omega0^2]);
bode(Tp, {1e1, 1e6})

%% Duty Cycle-to-Inductor Current Transfer Function Tpi
Tpix = (-Vo*(RL+rC*D*rC))/(D*L*(RL+rC));
Tpi0 = -Vo*(1+D)/(D*r+RL*(1-D)^2);
omegazi = (1+D)/(C*(RL+rC+D*rC));
fzi = omegazi/(2*pi);
Tpi = Tpix*tf([1 omegazi], [1 2*zeta*omega0 omega0^2]);
bode(Tpi, {1e1, 1e6})

%% Transfer Function of Filter and Non-inverting Amplifier Tf
%normally 50% attenuation @ fs -> ftp = 0.575*fs
fpf = fs*sqrt((phitp^2)/(1-phitp^2));
Cf = 1/(2*pi*fpf*Rf);
```

```
omegapf = fpf*2*pi;
Tf = tf(1, [Rf*Cf 1]);
bode(Tf, {1e1, 1e6})

%% Transfer Function of Pulse-Width Modulator Tm

Tm = 1/VTm;
VCI = D*VTm;

Rs = (VCI-VOFF)/IL;
%[Rs] = V/A = currentsensor gain

%% Uncompensated Loop Gain Tki

Tki0 = (Rs/VTm)*(-Vo*(1+D))/(D*(r+RL*(1-D)^2));
Tki = Tm*Tpi*Rs*Tf;
bode(Tki, {1e1, 1e6})

%% Transfer Function of Control Circuit for Inner-Current Loop Tci

omegac = fci*2*pi;

% Tkifc = 1.3228;
% PhiTkifc = -95.4;
[Tkifc,PhiTkifc] = bode(Tki,omegac);

phimi = PMi-PhiTkifc-90;

K = tand(phimi/2 + 45);

C2i = Tkifc/(omegac*K*R1i);
C1i = C2i*(K^2-1);
R2i = K/(omegac*C1i);

Tcio = 1/(R1i*(C1i+C2i));
omegazci = 1/(R2i*C1i);
omegapci = (C1i+C2i)/(R2i*C1i*C2i);

Tci = Tcio * tf([1/omegazci 1], [1/omegapci 1 0]);
bode(Tci, {1e1, 1e7})

%% Compensated Loop Gain of Inner-Current Loop Ti
Ti = Tki*Tci;
```

```
%Ti0 = (Rs/VTm)-((Vo*(1+D))/(D*(r+RL(1-D)^2)))*(1/(R1i*(C1i+C2i)));
bode(Ti, {2e1, 1e7})

%% Reference Voltage-to-Inductor Current Transfer Function Ticl

Ticl = (Tci*Tm*Tpi)/(1+Ti);
bode(Ticl, {2e1, 1e7})

%% Reference Voltage-to-Output Voltage Transfer Function Tpicl

Tpicl = (Tci*Tm*Tp)/(1+Ti);
bode(Tpicl, {2e1, 1e7})

%% Transfer Function of Feedback Network

beta = VRV/Vo;

%% Uncompensated Loop Gain Tkv

Tkv = beta * Tpicl;
bode(Tkv, {1e2, 1e7})

%% Transfer Function of Control Circuit for Outer-Current Loop Tcv

omegacv = fcv*2*pi;

[Tkvfc,PhiTkvfc] = bode(Tkv,omegacv);
PhiTkvfc = PhiTkvfc-360;

phimv = PMv-PhiTkvfc-90;

Kv = tand(phimv/2 + 45);

C2v = Tkvfc/(omegacv*Kv*R1v);
C1v = C2v*(Kv^2-1);
R2v = Kv/(omegacv*C1v);

% C2v = 700e-9;
% C1v = 3.5e-9;
% R2v = 324e3;13.56u


Tcvo = 1/(R1v*(C1v+C2v));
```

```
omegazcv = 1/(R2v*C1v);
omegapcv = (C1v+C2v)/(R2v*C1v*C2v);

Tcv = Tcvo * tf([1/omegazcv 1], [1/omegapcv 1 0]);
bode(Tcv, {1e1, 1e7});

%% Compensated Loop Gain Tv

Tv = Tkv*Tcv;
bode(Tv, {1e2, 1e7});

%% Reference Voltage-to-Output Voltage Transfer Function Tpcl

Tpcl = (Tcv*Tpicl)/(1+Tv);
%bode(Tpcl, {1e2, 1e7});

%% Print Values

C1i
C2i
R2i

C1v
C2v
R2v
```

Listing 3: Average Current-Mode Regulator Calculations

```
% based on snva555
% https://www.ti.com/lit/an/snva555/snva555.pdf

%% Parameters

Vin = 5;
Vo = 5;
Ro = 25;
fs = 1000e3;

Ci = 10e-6;

L = 47e-6;
Rl = 100e-3; % Inductor series resistance
```

```
15
16 Gi = 20;
17 Rs = 100e-3; % Shunt resistor
18
19 Co = 20e-6;
20 Rc = 100e-3; % Output capacitor series resistance
21
22 fc = 30e3; % Crossover frequency
23 omega_fc = fc*2*pi;
24
25 PM = 60;
26
27 Io = Vo/Ro;
28
29 Q = 2/pi;
30
31 VRamp = 3; % V
32
33 Gv = 3300; % 70 dB
34 GBW = 10e6;
35
36 gm = 13.56e-6;
37 R1i = 1/gm;
38
39 T = 1/fs;
40
41 %% Linear Model Coefficients
42 Vap = Vin + Vo;
43 D = Vo/(Vin+Vo);
44 D_= 1-D;
45 R = Vo/Io;
46
47 %% Buck-Boost Design Example - Control-to-Output
48 Ri = Gi * Rs;
49 Vsl =Vo*Ri*(T/L);
50
51 Km = 1/((0.5-D)*Ri*(T/L)+(Vsl/Vap));
52 K = 0.5*Ri*(T/L)*D*D_;
53 KD = 1+(Ro*D)/R+((Ro*D_^2)/Ri)*(1/Km+K/D_);
54
55 vo_vc = (Ro*D_)/(Ri*KD);
56 vo_vc_dc = 20*log10(vo_vc);
57
```

```
omega_p = KD/(Co*Ro);
omega_z = 1/(Co*Rc);
omega_r = (R*D_^2)/(L*D);
omega_L = (Km * Ri)/L;
omega_n = omega_L/Q;

fp = omega_p/(2*pi);
fz = omega_z/(2*pi);
fr = omega_r/(2*pi);

fl_Q = (1/(4*T*Q))*(sqrt(1+4*Q*Q)-1);

tf_p = tf(1,[1/omega_p 1]);
tf_r = tf([(-1/omega_r) 1], 1);
tf_z = tf([1/omega_z 1], 1);
tf_n = tf(1,[1/(omega_n^2) 1/(omega_n*Q) 1]);

%% Uncompensated Loop Gain
vo_vc_tf = ((Ro*D_)/(Ri*KD))*tf_r*tf_z*tf_p*tf_n;

%subplot(2,1,1);
bode(vo_vc_tf, {1e1, 1e7})



%% Transfer Function of Control Circuit for Outer-Current Loop
[Gfc,Phifc] = bode(vo_vc_tf,omega_fc);

Phifc = Phifc-360;
PM_max = 180 + Phifc
phim = PM-Phifc-90;

K = tand(phim/2 + 45);

%R1i = 3740;
C2i = Gfc/(omega_fc*K*R1i);
C1i = C2i*(K^2-1);
R2i = K/(omega_fc*C1i);

%  R1i = 3740;
%  C2i = 10e-12;
%  C1i = 6.8e-9;
%  R2i = 8.2e3;
```

```
101
102 Tcio = 1/(R1i*(C1i+C2i));
103 omegazci = 1/(R2i*C1i);
104 omegapci = (C1i+C2i)/(R2i*C1i*C2i);
105
106 Tci = Tcio * tf([1/omegazci 1], [1/omegapci 1 0]);
107 %subplot(2,1,2);
108 bode(Tci, {1e1, 1e7})
109
110 %% Compensated Loop Gain Tv
111 %subplot(3,1,3);
112 bode((Tci*vo_vc_tf), {1e1, 1e8})
113
114 %[fc_real, phi_real] = bode((Tci*vo_vc_tf), omega_fc)
115
116 %% Print Values
117
118 C1i
119 C2i
120 R2i
121
122
123
```

Listing 4: Peak Current-Mode Regulator Calculations