Design of a Fully Integrated Buck-Boost Converter ASIC

A small buck-boost converter ASIC with integrated switches on a commercial 0.35 um process node for use in a charging case for hearing devices

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Abstract

This document presents the results of a project aimed at designing an Application Specific Integrated Circuit (ASIC) for a charging cradle for Hearing Instruments (HI) from Sonova AG. The main objective of the ASIC was to safely charge the HI from a standard USB power supply. The ASIC was designed to charge two HIs simultaneously at their maximum charging speed, and included a serial port for external configuration.

The project was divided into two phases: the pre-layout phase which was already documented in the previous year and the post-layout phase. The pre-layout phase involved creating the specifications and a system design with ideal components. These components were then replaced with implementable designs from libraries or custom-made designs, while still meeting the specifications. The post-layout phase involved creating a layout for the ASIC, manufacturing and packaging the chip, and validating and characterizing the samples.

The results of the project showed that the ASIC mostly worked as intended, with some limitations. The chip was able to meet the tape-out deadline, and the test setup created for the project allowed for testing of the samples. The automated tests and manual measurements provided valuable insights into the performance of the chip. However, there were some issues with the current measurement circuit and the default register configurations. Despite these issues, the high-level functionality of the chip was preserved, and a large set of the planned tests were completed.

Acknowledgements

We would like to express our sincere gratitude to our advisor, Lars Kamm, for his guidance and support throughout this project. His expertise and insights were invaluable in helping us navigate the complexities of ASIC design. We would also like to thank the team at OST Rapperswil for providing us with the resources and environment necessary to carry out this project.

Contents

1 Assignment

1.1 Introduction

The goal of this project is to create a prototype ASIC to be used inside a charging cradle for HI from Sonova AG. The main objective for the ASIC is to safely charge the HI from a standard USB power cable. Since there are two HI in a cradle, it must be possible to charge both HI simultaneously at their maximum charging speed. There should be a serial port to read and write data to the chip, in allow for external monitoring and configuration.

In a first step the specification shall be created and a system design proposal with ideal components should be designed and simulated. To make the chip manufacturable, these ideal components shall one by one be replaced with implementable designs from libraries or custom made, while still being able to meet the specifications. Based on the system design a layout shall be created in such a way that an ASIC can be manufactured.

Once the ASIC has been manufactured and packaged, the chip shall be validated and characterized. The measured specifications shall be compared with the requirements.

1.2 Technical Requirements

The main technical requirements of the ASIC concern the charging of the HI. The ASIC should provide a constant voltage of 5 V off of a Universal Serial Bus (USB) power supply, which can have a wide voltage range of 4.3 V to 5.3 V. As the input voltage can be higher or lower than the output, the charger must be able step up as well as step down the voltage.
Each HI can pull a maximum charging current of 80 mA, the chip therefore needs to be able to supply around 100 mA per output, in order to have some margin. Additional functionalities and safety features are allowed but not a must.

Input Voltage Range	4.3 V - 5.3 V
Output Voltage	4.9 V-5.1 V
Output Current	200 mA

Table 1: *Main requirements for the charger ASIC*

The full technical requirements can be found in the attachments.

1.3 Background of Application

The project idea originally came from Sonova AG, therefore most of the requirements were provided by them. Since the scope of the requirements is large and it's not possible to fulfil all of them in the given time and with the given resources, the focus shall be on the basic functionalities mentioned above.

1.4 | Scope of Work

1.4.1 | Project Thesis 1

- Literature study
- Specifications
- Verification
- Design for test

1.4.2 | Project Thesis 2

- Layout
- Post Layout Simulations
- Tape out
- Validation plan
- PCB for validation
- Validation
- Test report

1.5 | Goals

- Getting familiar with the various tools required for ASIC design
- Document the project and provide reasoning for important design decisions
- Understand and complete the entire ASIC design flow consisting of:
  - System design
  - Layout
  - Tape out
  - Validation

1.6 | Mile stones

- Project start: 23.09.2022
- System Design: 14.07.2023
- Delivery of report 1: 14.07.2023
- Presentation one 10.07.2023
- Tape out ready: 03.11.2023
- Delivery of report 2: 11.07.2024
- Presentation two 11.07.2024

1.7 | Organization

- Advisor: Lars Kamm
- Work place: OST Rapperswil, room 8221
- Meetings: every two weeks
- Document filing: \\hsr.ch\root\auw\sge\studarbeiten\MikroelSys\MSE\MSE_22HS_-Jansky_Meyer

2 Introduction

The goal of this project was to create prototype ASIC for use inside a charging cradle of a hearing aid. It solves the problem of creating a stable and accurately regulated 5 V from any USB specification compliant power source. This entails being able to boost the input voltage up from 4.35 V as well as being able to buck it down from 5.5 V and regulate to a stable 5 V from any voltage in between. This requirement comes from the fact that modern HI's have a lithium battery inside, which have a charging cut-off voltage of 4.2 V. In the case with a 4.35 V supply voltage and the use of an Low Drop-Out (LDO) regulator to charge with battery, the dropout voltage of the regulator can not be maintained leading to a loss of output regulation. Therefore the battery will not be able to be fully charged or could only be charged at a reduced rate. The resistive losses stemming from the contact resistances of the charger pins further increase the headroom required. A stable voltage is therefore required to charge the HI at full speed, as the contact resistances can be in the order of several ohms, which causes a significant voltage drop. [1]

The project of designing and testing such an ASIC was divided in two parts, a „pre-layolut phase“ and a „post-layolut phase“, since the project was executed in a master program which requires two separate stages. This report will focus on the „post-laylout phase“ as the „pre-layolut phase“ was already documented in the previous report. In the first chapter we represent parts of the tape-out process with an emphasis on the design changes since the last report and a high-level overview of the designed Integrated Circuit (IC). Thereafter we present the test setup created in order to validate the design. The test setup contains custom Printed Circuit Board (PCB)s for the characterization and custom software for automated testing. We used the test setup to characterize the samples we received and present the results in the subsequent chapter. Where applicable comparisons are made between the simulated results and the real world hardware. In the last chapter we go in depth into the limitations with the chip we discovered and provide analysis of the root cause.

3 Tape-Out

The initial objective was to conclude the chip design phase of this project within the scope of the first project thesis. Unexpected delays in the timeline however led us to miss the initial tape-out deadline. A substantial portion of this delay stemmed from the necessity to overhaul the buck-boost converter regulator loop. The regulator loop previously implemented average current-mode control which necessitates stringent requirements for the current measurement circuit. As a result, the design was altered to implement peak current-mode control as is has more manageable requirements for the current measurement. Despite the provision of an extended timeline, finalizing the design before the deadline remained a challenging task requiring the removal of some nonessential features in oder to meet the deadline.

3.1 Buck-Boost Converter

The layout of the buck-boost converter can be seen in Figure 1 with annotations showing the rough floorplan of the circuit. Surrounding the converter are the four large switching transistors that significantly increased in size between initial planning in the previous thesis and to what was ultimately implemented. The exact values and sizes are listed in Table 2 and Table 3. The largest contributor to the losses in the power-stage surprisingly are the metal trace resistances which increased the theoretical $R_{DS,on}$ of the P-type Metal-Oxide Semiconductor (PMOS) power transistors from 58.3 mΩ to an effective value of 240 mΩ in post-layout simulations. These metal resistances could not be reduced through wider traces as the maximum metal density for manufacturing was the limiting factor.
The large empty space above the error amplifier in Figure 1 was initially intended for a temperature sensing circuit in order to measure the rough temperature of the power electronics and to disable operation in case of an over temperature event. Due to the tight timeline, the layout of this circuit was not completed as the priority was shifted towards finishing other more critical circuits. As a result of the same issue the implementation of Design For Testing (DFT) functionality was kept to a bare minimum and only includes the ability to measure the oscillator clock frequency, the bandgap reference voltage and the internal current reference. Consequently, the chip is with respect to troubleshooting a black-box with no possibility to measure some important internal signals.

Characteristic	Planned Value	Implemented Value
Typ. $R_{DS,on}$	113 mΩ	58.3 mΩ
# of Transistors	4834	9408
Width	96.7 mm	188.2 mm
Size	1000.2 µm x 486.8 µm	1228.8 µm x 764.4 µm

Table 2: *Specifications of the power PMOS*

Characteristic	Planned Value	Implemented Value
Typ. $R_{DS,on}$	72.8 mΩ	37 mΩ
# of Transistors	2800	6080
Width	56 mm	121.6 mm
Size	641.4 µm x 483.1 µm	972.8 µm x 688 µm

Table 3: *Specifications of the power N-Type Metal-Oxide Semiconductor (NMOS)*

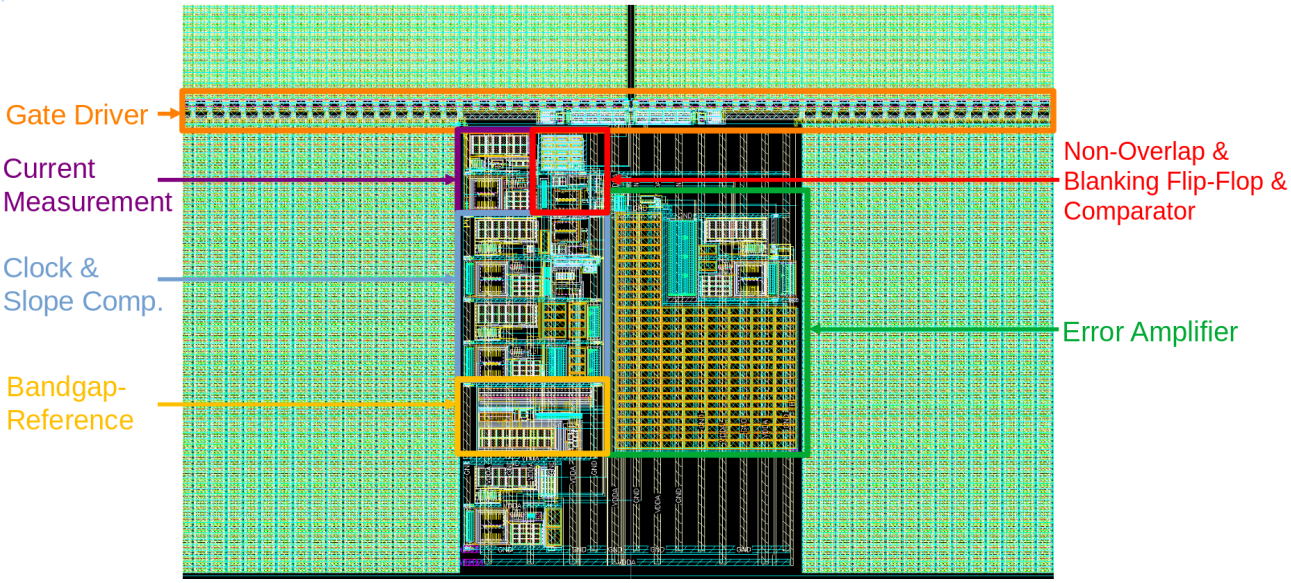

Figure 1: *Layout of the buck-boost converter regulator surrounded by the large power stage transistors*

3.2 Overall Chip Floorplan

As can be seen in Figure 2, this design is significantly pad limited as opposed to core limited. The entire lower right corner is unused and in general the lower third is sparsely populated. Conversely the upper two thirds is almost entirely filled the the buck-boost converter circuit with the majority of the area taken up by the four large switching transistors. They were maximized in size to reduce conversions losses and even take up the majority of the entire chips area. A large number of pads were used in parallel for the converters input, output and switching nodes to meet the current handling requirements and not exceed the recommendation of 50 mA per pad. In the bottom left the digital circuitry for the Serial Peripheral Interface (SPI) periphery and internal registers can be seen as well as supporting circuitry like the Power-on-Reset (POR) and bandgap voltage reference.

Property	Value
Function	Buck-Boost Converter
Package	QFN48 7x7 mm
Process	X-FAB 350 nm
Size	2712 µm x 2952 µm
Area	8.006 mm^2

Table 4: *ASIC Properties*

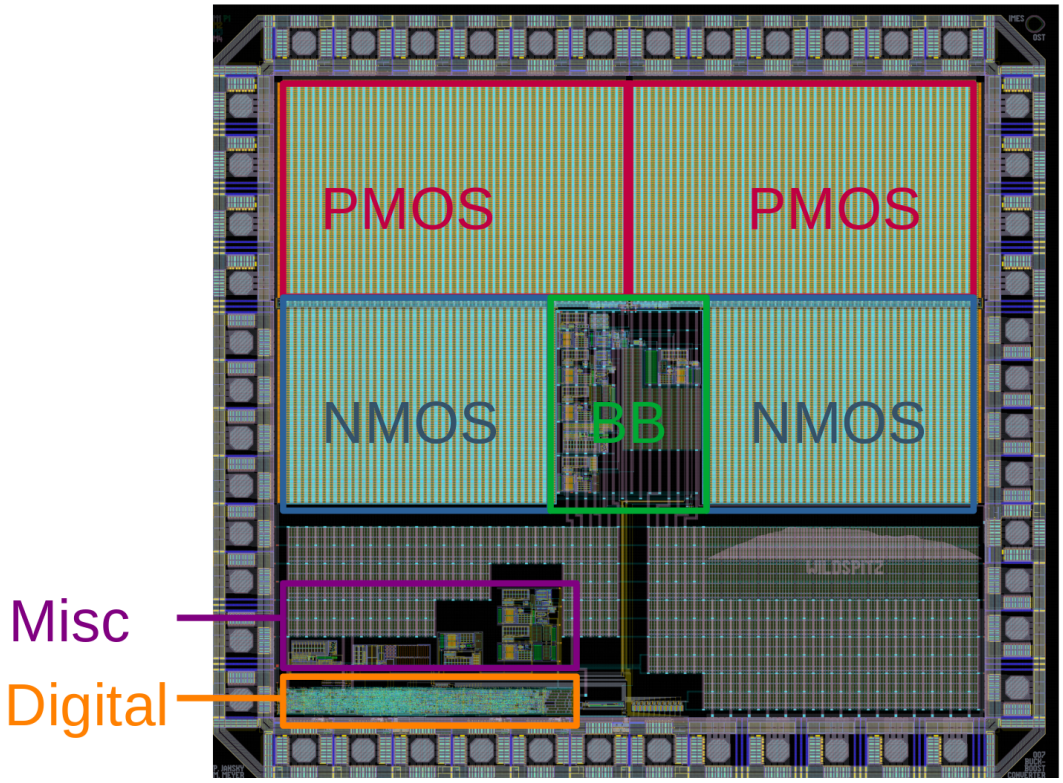

Figure 2: *Floorplan of the entire chip with annotations*

3.3 Package

In Figure 3, the QFN-48 package of the chip is illustrated with the pinout of the device marked. It is evident that there are two distinct ground connections, namely a power ground GND_2 for the switching converter and GND as a general purpose ground for the internal circuits. The same applies to the supply voltages with V_IN being the power input of the switching converter and VDD_L being the internal logic supply. While these two domains are independent and not internally connected, they typically would be connected together on the PCB. It is however advisable to separately bypass the power domains and separate them with a ferrite bead to minimize switching noise interfering on the logic supply. The full pinout can be seen in Figure 3.

- **A_OUT:** Analog test pin to mux out internal signals. See also subsection 5.1
- **D_OUT:** Outputs internal clock when enabled. See also subsection 5.1
- **FB:** Feedback to overwrite output voltage by external voltage divider
  $V_{OUT} = 1.25\,\mathrm{V} \cdot \frac{R_{FBT}}{R_{FBB}}$; $(R_{FBT} + R_{FBB}) \ll 100\,\mathrm{k\Omega}$
- **GND:** Ground of digital logic and internal circuits
- **GND_2:** Ground pins for DC/DC converter
- **L_IN/L_OUT:** Connection to an external 47 µH coil
- **RST:** Active high reset, resets the whole chip including the internal registers
- **SPI*:** SPI interface connections
- **VDD_L:** Supply of digital logic and internal circuits
- **V_IN:** Supply voltage for power stage
- **V_OUT:** Buck-boost converter output, nominally 5.0 V

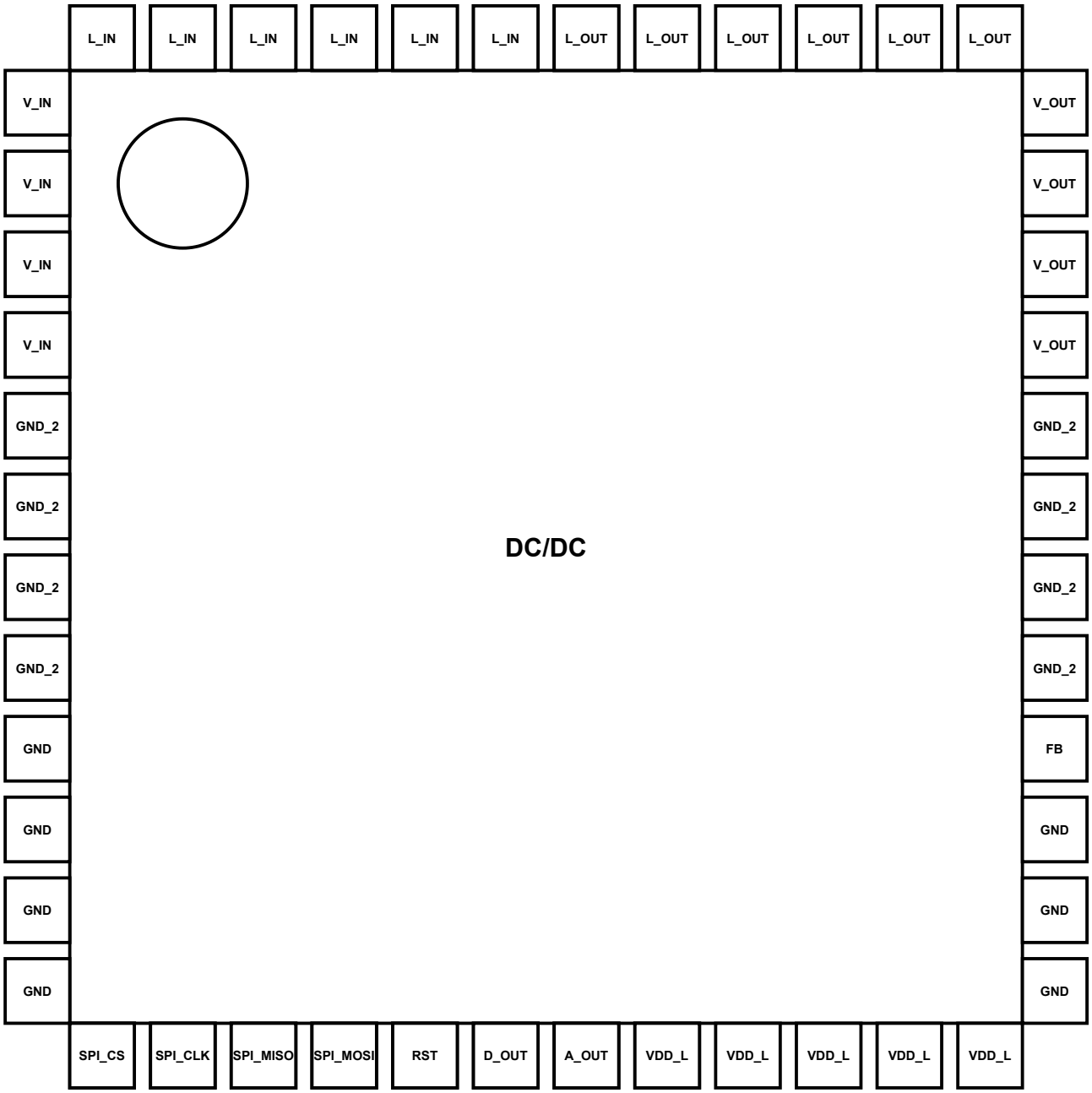

Figure 3: *QFN-48 Device Pinout, Top View*

4 Test Setup

4.1 Hardware

This section introduces the hardware setup created in order to validate our chip design and compare the received samples with the results obtained from simulations. For an as like to like comparison with the simulations as possible, the hardware tries to replicate the virtual test bench setup. As in the virtual setup, the physical setup contains electronically controllable loads to compare the dynamic regulation characteristics with the simulated results. The response to load steps also gives insight into the closed loop regulation characteristics like bandwidth and phase margin of the internal regulation loop. An additional goal is to verify our SPI slave implementation with a commercial SPI master device like an Arduino or USB to SPI converter. Of additional interest is the accuracy of internal signals such as the internal oscillator and the the bandgap voltage reference.
The hardware should allow for the following measurements:

- Line Regulation
- Load Regulation
- Output Voltage Regulation Accuracy
- Efficiency
- Startup Behavior
- Short Circuit Behavior
- SPI Functionality
- Internal Oscillator Frequency Accuracy
- Bandgap Voltage Reference Accuracy

Continuing the test bench analogy, the test setup is split into two components, a test bench like PCB we call the Adapter PCB and multiple smaller PCBs. These smaller PCBs only contain the Device Under Test (DUT) and a minimal amount of supporting components for its orderly operation. As these PCBs get plugged in on top of the Adapter PCB, we refer to them as Hats.

4.1.1 | Adapter PCB

The main Adapter PCB contains the functionality of the test bench and has a common plug-in location for the Hats. The Adapter is designed in such a way, that the DUT can be placed in the thermal chamber of the thermal airstream system TP04300A in order to test the DUTs functionality under various thermal conditions. Four electronically controllable load resistors are contained on the PCB for load step measurements and current sense amplifiers are used to measure the current flowing into and out of the switching converter. In order to verify the SPI communication with the DUT, there are headers and voltage translators for communication with either an Arduino Nano Every or an FTDI FT232 based USB to SPI adapter.

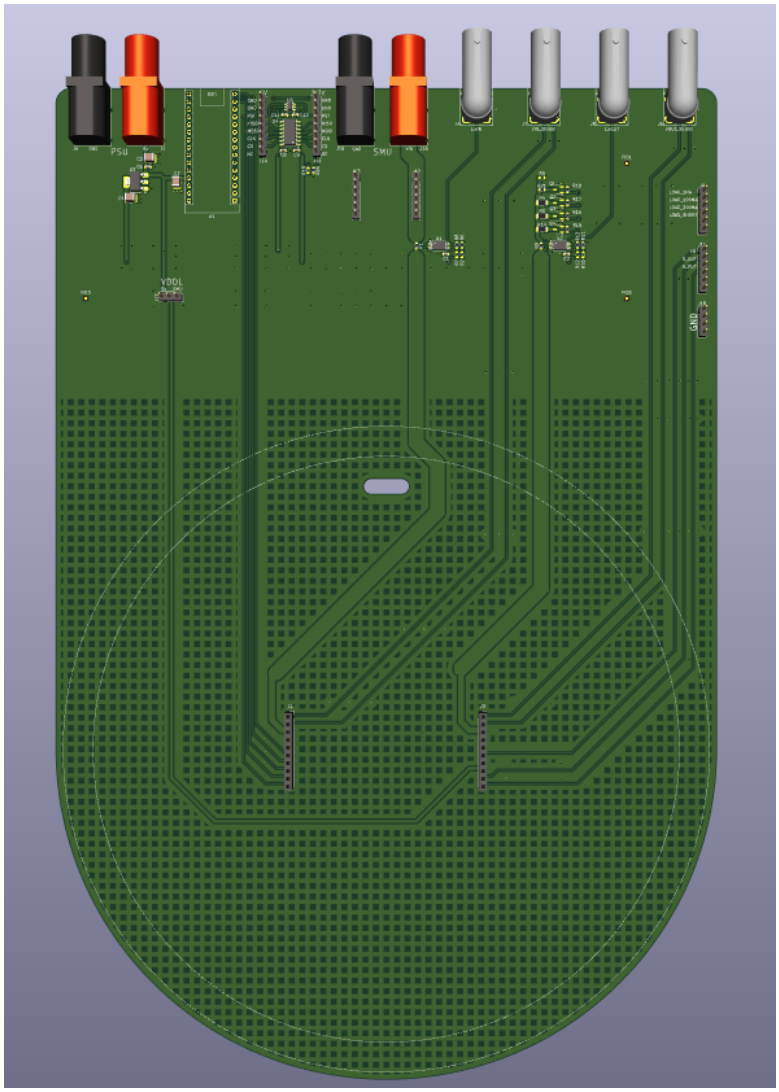

Figure 4: *3D render of the Adapter PCB, the design files can be found in the following git repository [2]*

4.1.2 | Hat PCBs

In total three different Hat PCBs were created in order to test various DUTs. One PCB contains a commercially available IC and the two other PCBs are intended for our manufactured chip. On the first PCB our chip is placed into an IC socket and in the second one the QFN package soldered directly to the board. The socketed version allows for the quick characterization of multiple samples and measurement of the variance of characteristics over the batch. The socket however introduces higher lead resistances and inductances as well as thermally isolates the chip from the PCB. The thermal isolation could lead to increased temperatures in high load conditions and in a worst case scenario could lead to damage of the chip. In practice however, no a measurable difference in characteristics was observable based on if the chip was socketed or not.

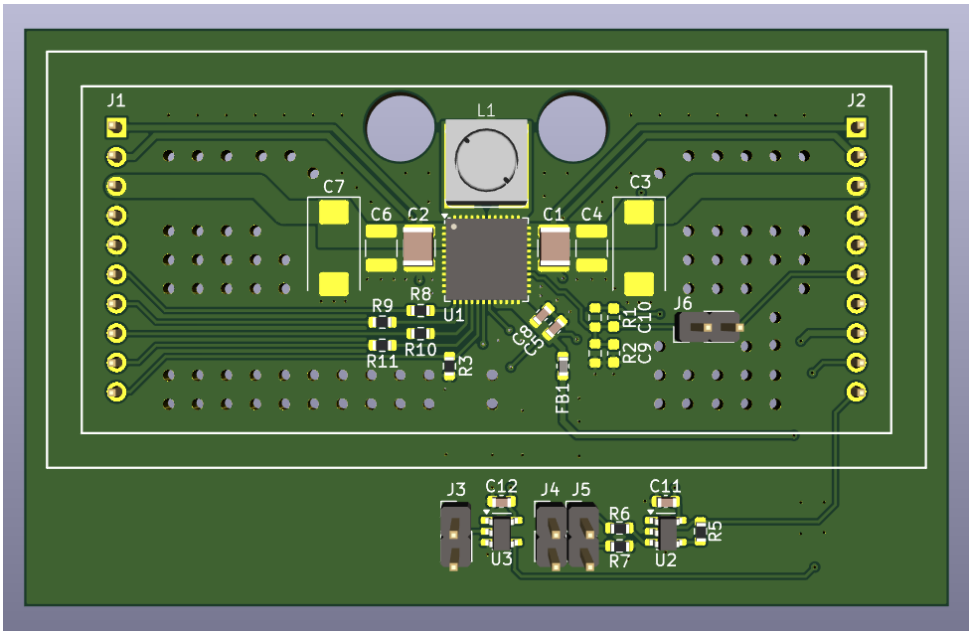

Figure 5: *3D render of the Hat PCB with the QFN package soldered to the PCB, the design files can be found in the following git repository [2]*

The reasoning to create a Hat with a commercially available chip was two fold. First it allows validation of the test setup with a real hardware before receiving samples and secondly it creates a baseline to compare our design against. For the commercially available IC we used the TPS63900 from Texas Instruments. While this IC is significantly smaller in physical size, it has a similar input and voltage range as well as current drive capabilities. Similarly it is also a highly integrated buck-boost converter with integrated switches in the standard cascaded-buck-boost converter topology. Nonetheless the TPS63900 has a significantly higher efficiency, greater than 90 %[3], as it is designed for ultra low-power applications and implements multiple advanced power saving features like dynamic switching frequency adjustment based on load conditions[3]. The chip additionally employs a novel drive scheme of the power stage leading to trapezoidal inductor current, as opposed to the traditional triangular waveform, which again leads to higher efficiency and to only a single operating mode over the entire input and output voltage range[3].

4.2 | Software

4.2.1 | Architecture

The architecture of the test software was designed with a modular approach in mind, incorporating separate classes for each test and measurement instrument. This design choice not only simplifies the extension of the software with new instruments and tests but also enables looping over different tests without the constant need to initialize and close measurement instruments.

For the data storage a database solution was selected providing for a convenient method for storing information and easily allowing for subsequent data analysis. SQLite was selected as the database of choice due to its lightweight nature and user-friendly interface, eliminating the need for a running server.

The database was structured with the following columns:

- **Id**: The unique identifier for each measurement
- **chip_id**: The identifier for the chip that was measured
- **measurement_type**: The type of measurement performed
- **parameter1**: The first parameter used for the test, such as the input voltage applied
- **parameter2**: The second parameter used for the test, such as the load applied to the output
- **temperature**: The temperature of the chip during the measurement
- **data**: The measured data
- **measurement_result**: The result of the measurement, if applicable
- **Timestamp**: The timestamp of the measurement

4.2.2 | Test Software Language

The test software was implemented using Python. Python is a high-level programming language widely utilized in the scientific community and increasingly in testing due to its ease of learning and the availability of drivers for nearly every measurement instrument [4]. Additionally, one of the authors had prior experience in writing test scripts in Python for chip verification and validation, enabling the initiation of test writing without a significant investment in learning a new programming language and environment.

4.2.3 | Test Software Implementation

Prior to commencing the test software development, the various tests to be performed were determined, aiming to align with those conducted in simulations. These included:

- Startup behavior with reset disabled
- Startup behavior with active reset and subsequently disabled reset
- Load step response with load variations of 1 mA, 100 mA, and 200 mA
- Output response to stepped input voltage changes
- Turn-off and turn-on behavior with brief reset enablement
- SPI test to mux out the wanted analog/digital signal, change the clock frequency, and read back the register values

4.2.4 | Test Setup

The primary test setup utilized the PXI system from National Instruments (NI). This system integrates various measurement instruments into a single unit and serves as the computer running the Python code. Consequently, there are minimal delays due to additional wires between the computer and measurement instruments. Moreover, synchronized triggers are available on this measurement system, eliminating the need for trigger wiring between instruments. This advantage reduces setup complexity and wiring requirements. The specific PXI system employed was the PXI model „NI PXIe-8881“, equipped with the following modules:

- **PXIe-4141**: This is a SMU (Source Measurement Unit) which can be used to apply the input voltage to the chip
- **E3631A**: This is a power supply which can be used to apply the input voltage to the chip
- **PXI-5142**: This is a two channel oscilloscope used to measure the output and input voltage of the chip
- **PXI-5163**: This is a two channel oscilloscope used to measure the output and input current of the chip
- **TP04300**: This is the thermostreamer used to control the temperature of the chip
- **PXI-6363**: This is a GPIO controller used to control the reset of the chip and the different load resistors
- **NGE-100**: This is a power supply to provide the power for the test circuit
- **FTDI C232HM-DDHSL-0**: This is a USB to SPI converter used to communicate with the chip

An overview of all the instruments can be seen in Figure Figure 6. More details about the hardware can also be found in the git repository[1] where test was written.

4.2.5 | Github

The test software was written using Git as its version control system, with the repository being hosted on GitHub. This choice was driven by GitHub's widespread adoption and its seamless integration for collaborative code sharing among team members. Furthermore, Git's robust features allow for efficient tracking of changes and management of various software versions. The repository can be found at the following link[2]. Additionally the repository uses github actions to automatically run tests on every push to the repository. This ensures that the code is written in a appealing way according to the PEP8 standard and that the tests are most probably running without any errors, for that flake8 and pylint were used as linter and integrated in the github workflow.

4.2.5.1 | Pylint

Pylint is a static code analysis tool for Python, adhering to the style guidelines outlined in PEP 8. It checks various aspects of Python code, including line length, variable naming conventions, and interface implementation consistency. Pylint is similar to Pychecker and Pyflakes but offers additional features such as generating UML diagrams using the Pyreverse module. It can be used independently or integrated into various IDEs and editors like Eclipse with PyDev, Spyder, Visual Studio Code, Atom, GNU Emacs, and Vim[5].

[1] https://github.com/gstei/asic_validation.git
[2] https://github.com/gstei/asic_validation.git

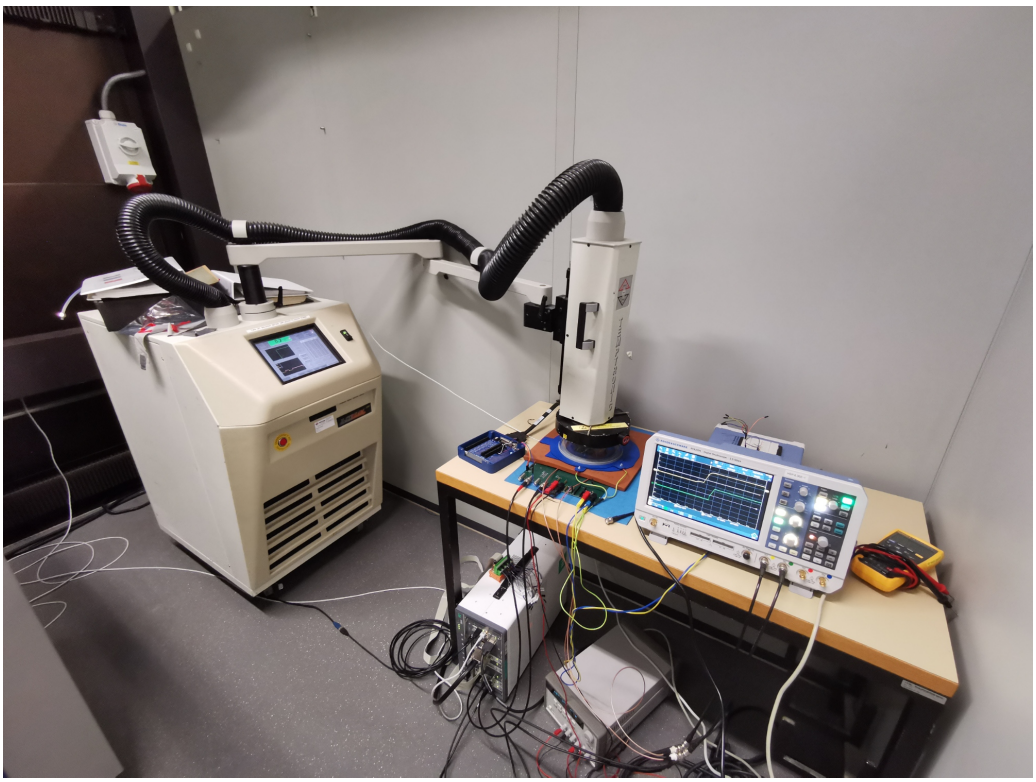

Figure 6: *Overview of the test setup*

4.2.5.2 | Flake8

Flake8 is a Python linting tool that scans Python codebases for errors, style inconsistencies, and complexity. It consists of three underlying tools: PyFlakes for error checking, McCabe for complexity analysis, and pycodestyle for style conformity with PEP8 guidelines. Flake8 stands out due to its extensive plugin ecosystem, allowing users to augment its capabilities and address a wide range of issues and concerns in Python code[6].

4.2.6 | SPI Interface

The chip's registers are controlled via an SPI interface, necessitating an SPI Master. For the SPI master the FTDI C232HM-DDHSL-0 USB to SPI converter was chosen, primarily due to its user-friendly nature and the availability of Python drivers.

A discrepancy between the SPI mode 1 implemented on the chip and the SPI mode 1 on the FTDI Chip was however found. On the FTDI Chip, the CS and the first SPI clock edge are activated simultaneously, which was not the case on the test bench used in the simulation to verify the digital part of the chip. Due to its implementation, the finite state machine only operates correctly when the CS is activated before the first clock edge, as illustrated in Figure 7 (CPOL=0, CPHA=1).

To address this, we implemented a custom driver in software, which operates at 1kHz instead of 500kHz. Given that we only need to write/read seven different registers, this slower speed does not significantly impact the overall performance, and the difference is imperceptible to the human operator.

However, for future projects, we recommend considering the test instruments during the chip design phase to avoid such issues. The SPI interface should function correctly with a standard microcontroller

that uses the SPI standard, as shown in Figure 7, where the CS is activated before the first clock edge. However, it's important to note that there are some unique implementations of the SPI, as in the FTDI C232HM-DDHSL-0, which should also be considered during the design phase.

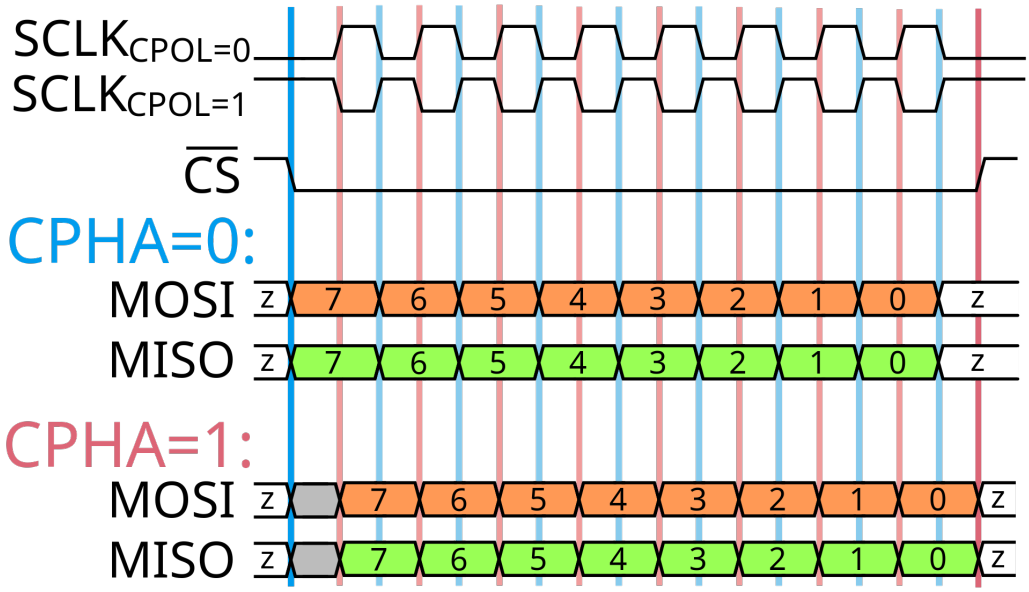

Figure 7: *SPI Modes [7]*

4.2.7 | Conclusion

In summary, one can say about the test scripts planned to validate the chip that it was a good decision to spend quite some time initially on how to set up the validation process and define what needs to be validated before actually writing the scripts. Due to that, a database was implemented and a linter integrated into the workflow early on, as mentioned earlier. This turned out to be a very good decision since once the tests were defined, the test scripts were written straightforwardly, and all the measurements were available in the database for further processing and plotting. Since the hardware was already available before the actual ASIC was in-house, one was able to use the spare time to implement all the test scripts and test them with another DC/DC converter from TI.

The only aspect that was not considered during this phase, but should have been, was what would happen if the ASIC does not work as expected. This turned out to be quite important although it would have been difficult to address since many things could go wrong. However, since the scripts were written in such a way that they did not allow for manual input, they could not be used directly, as our chip had startup difficulties and needed manual input, as mentioned in subsection 6.2, which was not covered in the test script implemented for the sample DC/DC chip.

Thus, in general, one can say that the best test script is useless when the chip does not work as expected. It fails, which is beneficial for detection, but does not provide the desired measurements. Therefore, in the end, we were not able to fully utilize the potential of the automation due to lack of time for adaption of the existing scripts, even though it was prepared and tested for the sample DC/DC converter from TI.

5 Results

On the SPI interface one should be able to successfully write and read back registers. Therefore a complete SPI driver was written in python which allows to simply mux out the wanted analog/digital signal, change the clock frequency and read back the register values. An overview of the registers can be found bellow Table 5 whereby register 2 does not exist as later elaborated on in subsection 6.1.

5.1 SPI Interface

Register	Function
0	stores the last spi command $< 7 : 0 >$
1	read only register with following value: b0=1, b1=0, b2=1, b3=0, b4=0, b5=0, b6=0, b7=0 <15:8>
3	analog mux $< 20 : 16 >$ 0=ground, 1=iboot ref, 2=vbgp, 3=output error amplifier, 4=ground, 5= ground
4	current limit tune $< 27 : 25 >$, current limit tune enable $< 24 >$
5	output voltage fb $< 32 >$
6	Freq tune digital part $< 42 : 40 >$ can add up to 3 caps eq sized caps to saw tooth ==> clock 4 times slower, dig out$< 47 >$ ==> enable clock on digital pad
7	Freq tune linear regulator$< 50 : 48 >$ can add up to 3 caps eq sized caps to saw tooth ==> clock 4 times slower

Table 5: *SPI register description*

Since the the SPI communication is working as in the testbench and the testscript is available in the git repository. No further test results are listed here. But one thing that one has to be aware of when one wants to control the chip is that the CS line has to be activated before the first clock edge arrives otherwise the communication will not work as mentioned in subsubsection 4.2.6.

5.2 POR

According to the simulation, the power-on reset (POR) exhibits the characteristics depicted in Table 6. The POR measurement was conducted on a single random sample at room temperature. To measure the characteristics from the simulation, a pull-up resistor was connected to the output of the analog test pin as the test pin exhibits high impedance when the chip is unpowered and is grounded when the chip is powered (as long as the analog test pint was not configured differently over the SPI). Consequently, when the chip gets powered and reaches a voltage over the minimum voltage of the POR, the analog test pin is driven to zero and this change is observable. Due to that it turned out that the minimum voltage of the POR is 3.72 V which is 0.02 V more than the upper corner of the Simulation. Since the time was limited and the deviation is very small no further investigations were made on that. The input and output delay where measured the same way and it turned out that those values are inside the corners of the simulations. For the input delay a value of 40 µs was measured which is the time from which the input voltage is over over 3.72 V and the analog test pin is driven

to ground. The other way around a value of 6.5 µs was measured as it can be also seen in Table 6 column four.

Description	Min.	Max.	Mes.	Unit
Input Delay	26	44	40	µs
Output Delay	4.4	6.8	6.5	µs
Current Consumption	13	31	-	µA
Min Voltage	3.176	3.7	3.72	V

Table 6: *POR characteristic*

5.3 Bandgap

The bandgap characteristics from the simulation can be seen in Table 7, Figure 8 and Figure 11. The measurements have thereby shown that the bandgap voltage is in the range of of the simulation, the mean value is just shifted by 10mV. As it can be seen in the comparison of Figure 10 and Figure 11. Furthermore due to the fact that the reference current is slightly to high the center of the bandgap vs temperature curve is not anymore at 40 °C but at about 55 °C as it can be seen in the comparison of Figure 8 and Figure 9. About the other parameters like the current consumption and the min voltage no measurements could be done since the band gap is not directly accessible.

Description	Min	Max	Unit
Bandgap Voltage	1.226	1.277	V
Current Consumption	16.73	23.53	µA
Min Voltage	2.3	2.9	V

Table 7: *Bandgap characteristic*

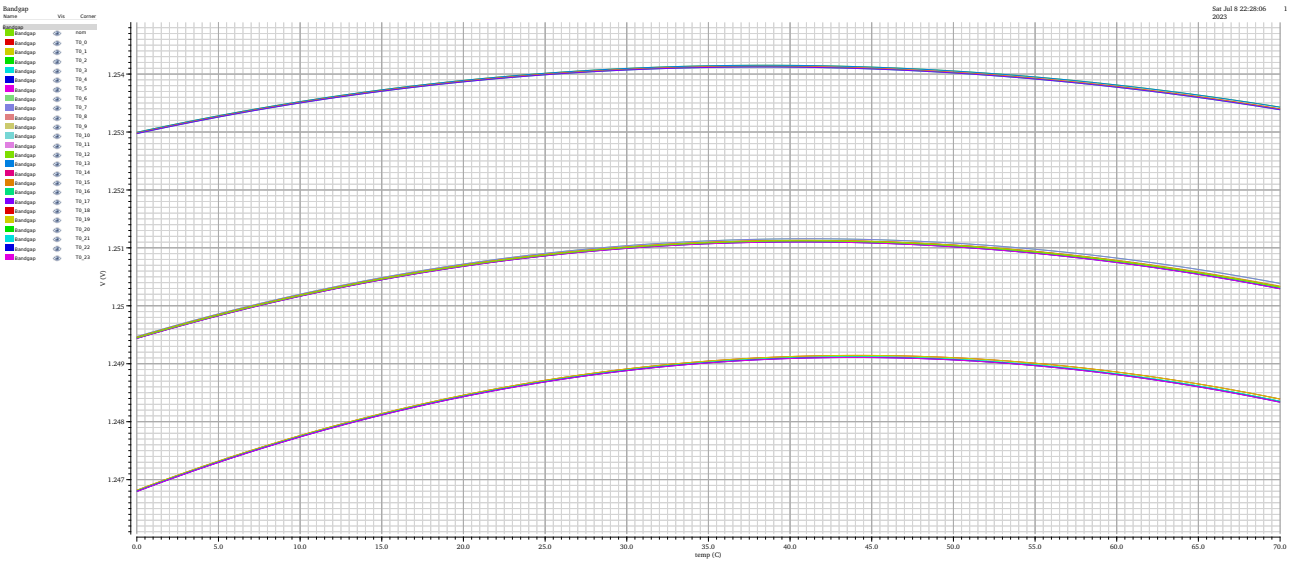

Figure 8: *Bandgap voltage vs temperature simulated*

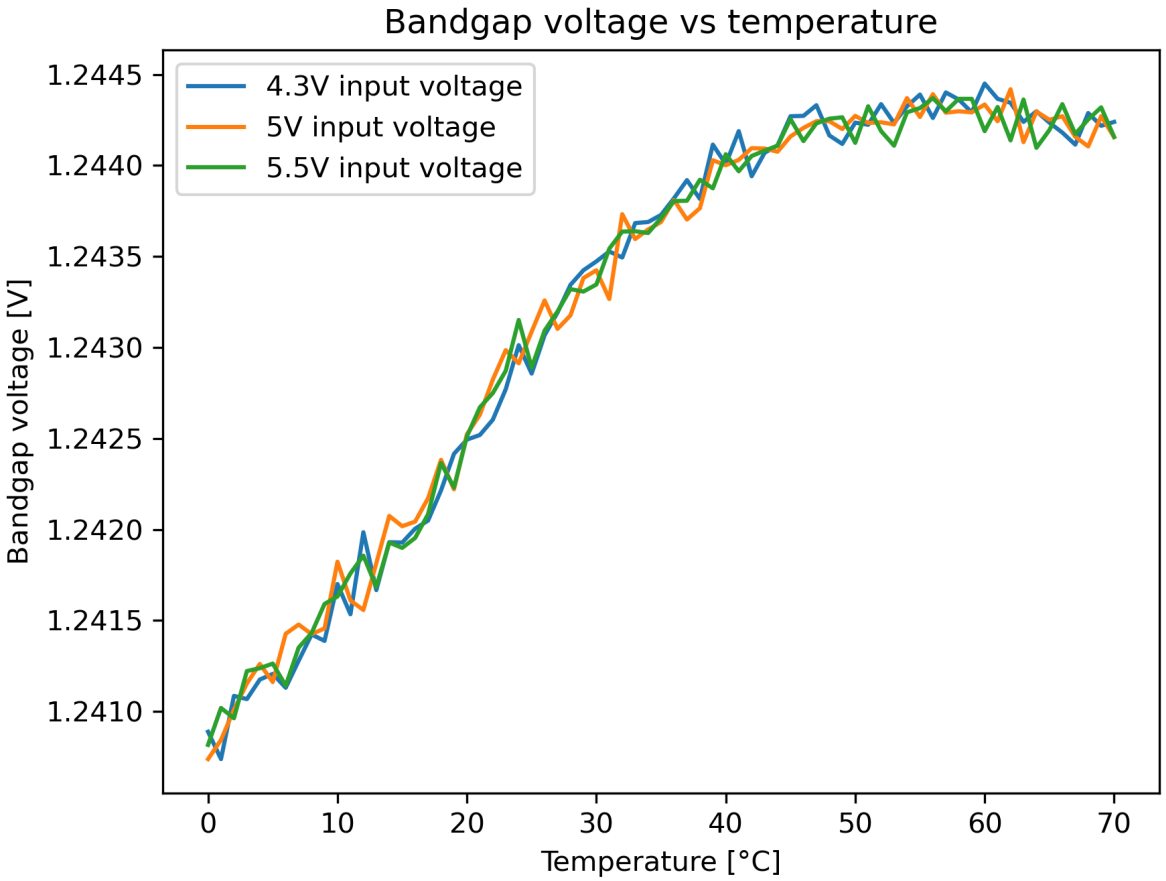

Figure 9: *Bandgap voltage vs temperature measured*

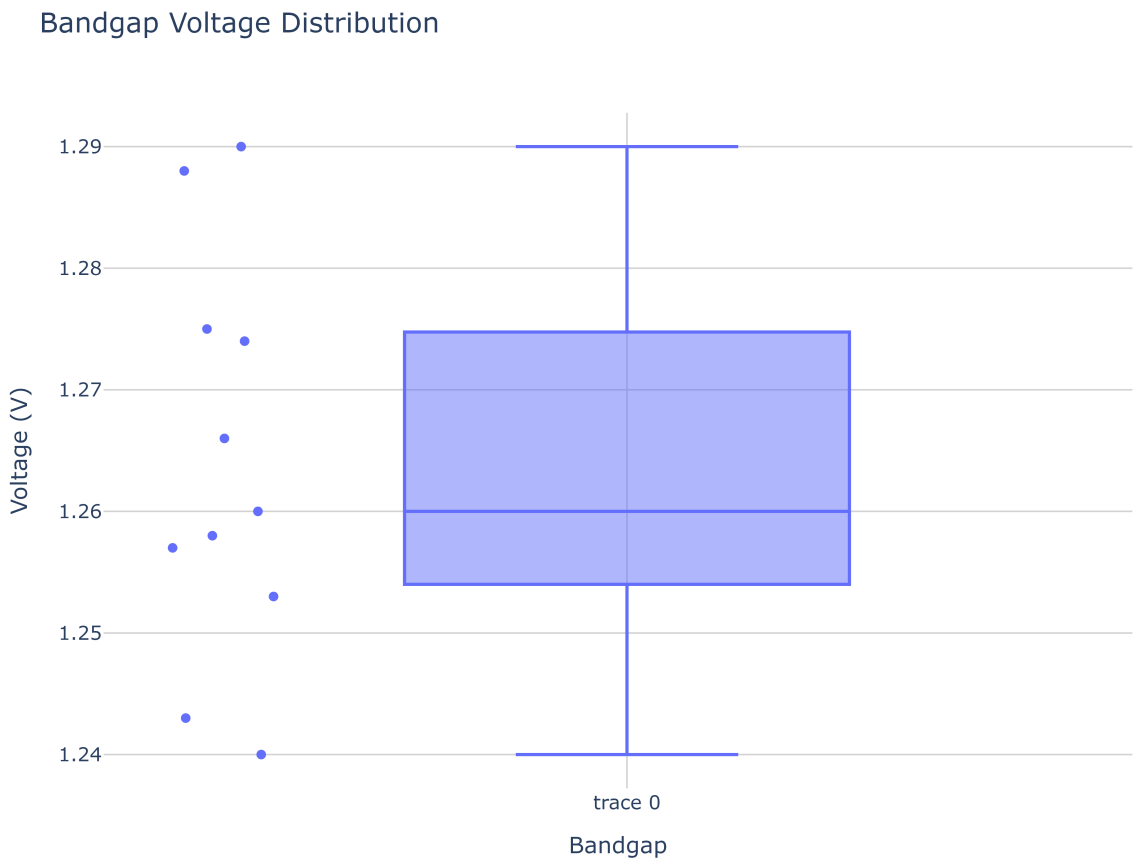

Figure 10: *Bandgap voltage distribution at 22 °C and 5V over different samples*

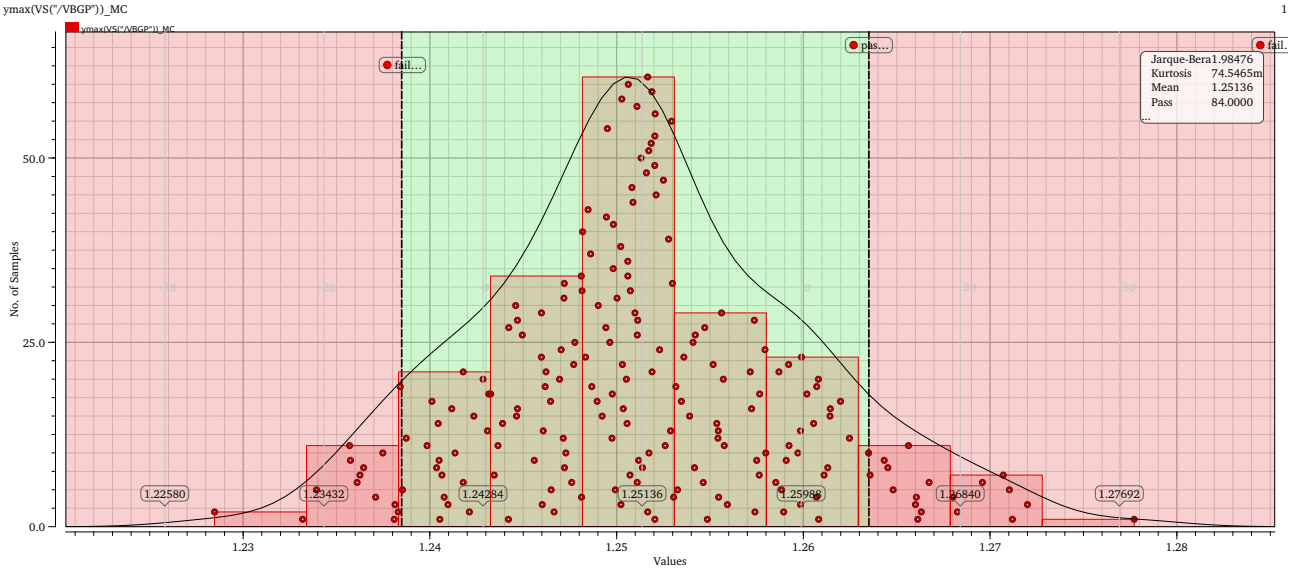

Figure 11: *Bandgap voltage Monte Carlo simulation (param.scs=3s, xh035.scs=mcg)*

5.4 Current Source

The current source characteristics from the simulation can be seen in Table 8 and Figure 12. The measurements have thereby shown that the current source is not in the range of the simulation. The current measured is about 4 µA higher than the one simulated which corresponds to a deviation of $\left|\frac{14.3\,\mu A - 10.3\,\mu A}{10.3\,\mu A}\right| \cdot 100 \approx 38.8\%$. An exact explanation for this behavior was not found, but since the oscillator has a similar deviation and is independent of the current source the deviation most probably comes from the „rnp1“ resistors since those were both used in the layout of the oscillator and the current reference. The current measured can be seen in Figure 13. About the other parameters no measurements could be done since the current source is not directly accessible.

Description	Min	Max	Unit
Reference Current	8.4	13.5	µA
Current Consumption	50	81	µA
Min Voltage (Threshold where $\frac{\Delta V_{in}}{\Delta I_{out}} > 1\,M\Omega$)	3	3.33	V

Table 8: *Current reference characteristics*

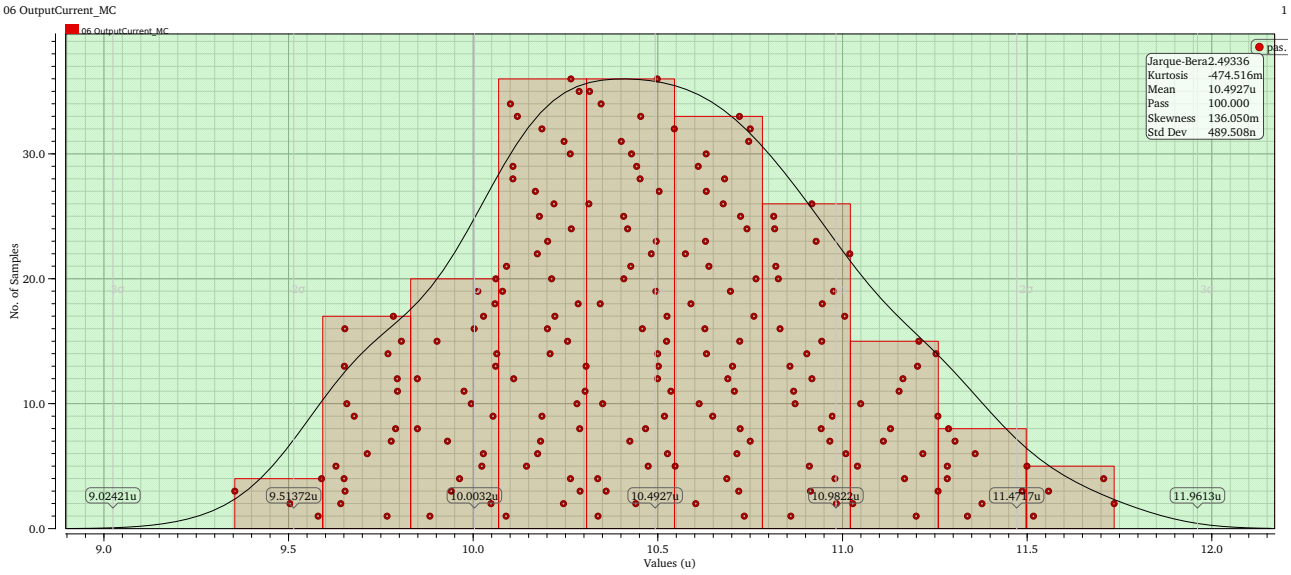

Figure 12: *Monte Carlo distribution of the current reference output current(param.scs=3s, xh035.scs=mcg)*

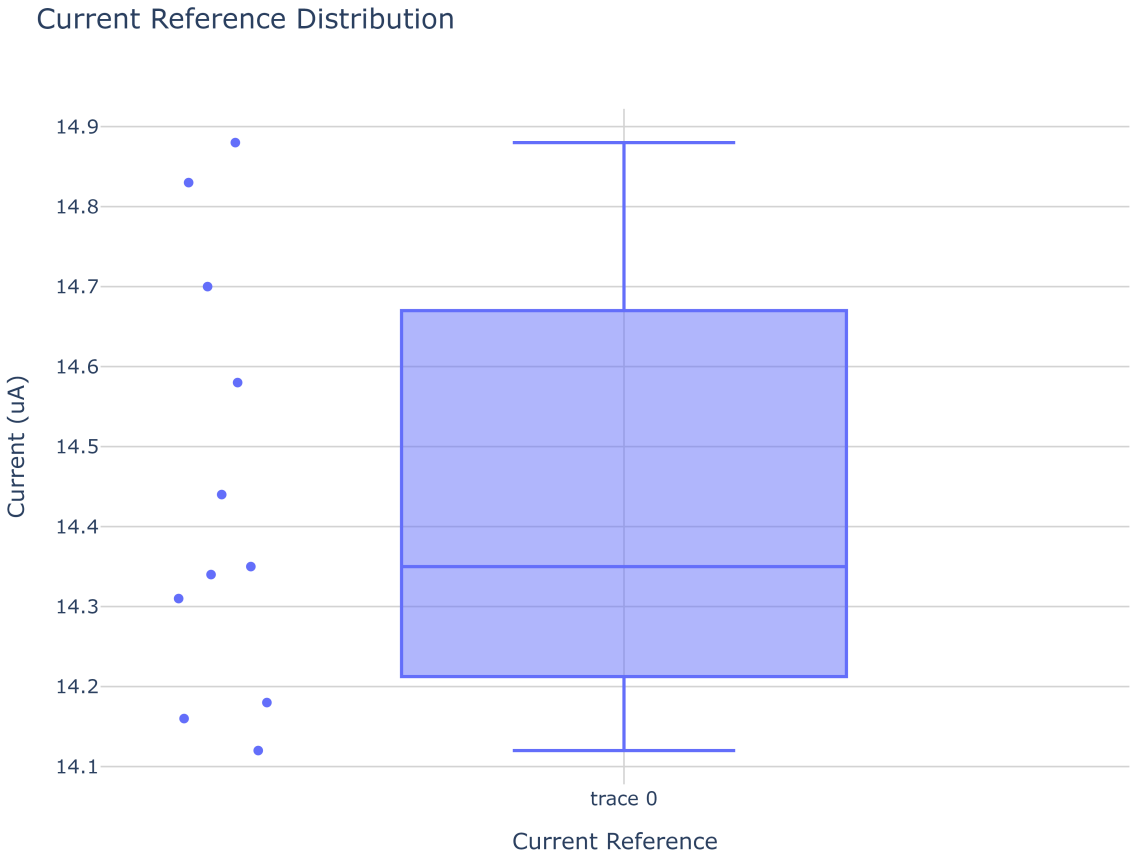

Figure 13: *Current reference distribution at 22 °C and 5V over different samples*

5.5 Oscillator

The oscillator characteristics from the simulation can be seen in Table 9. The measurements have thereby shown that the oscillator is not in the range of of the simulation, when there is no configuration made over the SPI one has a nominal frequency of 2.63 MHz, whereas in the simulation one had 1.7 MHz, which results in an deviation of $\left|\frac{2.63\,\text{MHz}-1.7\,\text{MHz}}{1.7\,\text{MHz}}\right| \cdot 100 \approx 54.7\%$, which is even more than in the current reference circuit. About the other parameters no measurements could be done since the oscillator is not directly accessible. Furthermore the frequency can also be tuned in the range of 1.17 MHz to 2.63 MHz over the SPI registers (measured values) which results in the frequencies which can be seen in Table 10.

Description	Min	Max	Unit
Frequency	1.15	1.8	MHz
Current Consumption	35	50	µA
Min Voltage	2	3.187	V

Table 9: *Oscillator specification simulated with default configuration (Register configuration 0)*

Register configuration	Frequency (kHz)
0	2630
1	2300
2	2190
3	1850
4	1670
5	1430
6	1270
7	1170

Table 10: *Measured frequency with different register configurations at* 22 °C *and* 5 V

5.6 | Buck-Boost Converter

5.6.1 | Start-up

The start-up behavior shows significant differences to the results observed in simulations. Instead of the expected gradual increase in the output voltage, the output voltage increases in distinct steps as can be seen in Figure 14. These distinct steps stem from the fact that the input voltage collapses cyclicly to under the limit given by the POR. The cycle can be described as the chip starting up and increasing the input current until the input voltage drops to below the limit given by the POR, thus disabling the chip and causing the input voltage to rise until the chip starts up again. The cycle continues until the output voltage reaches close to the nominal level and the outer voltage control loop regulates the inductor current down.
The underlying issue is a misconfiguration of the internal registers causing the current limit to be disabled on start-up and the converter increasing the inductor current to excessive levels, leading to the collapse of the input voltage. The cause is further elaborated on in subsection 6.3.

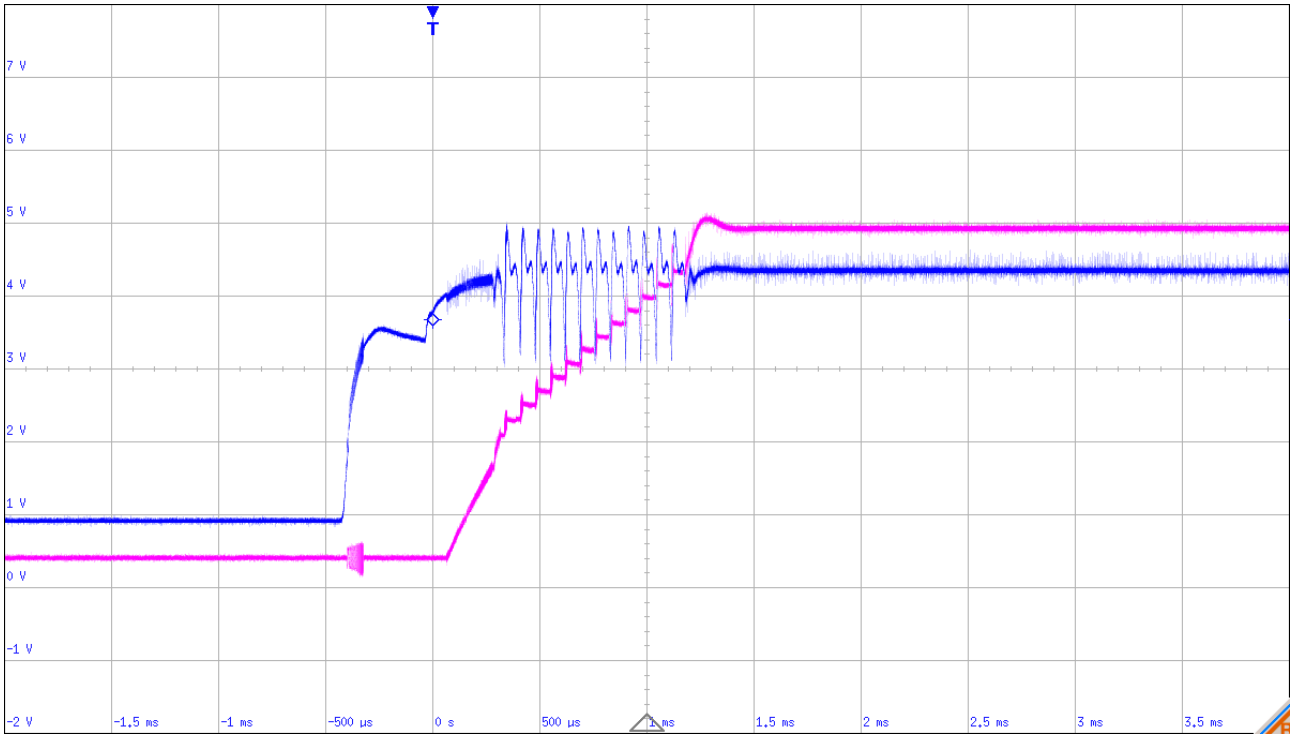

Figure 14: *Start-up behavior without an attached load. Dark Blue: V_{IN} measured; Pink: V_{OUT} measured*

5.6.2 | Load Step Response

The response to a load step is satisfactory and can be seen Figure 15. The regulation behavior is similar to the simulated response, with the caveate that the measured controller has a higher bandwidth as can be seen in the faster response. It is also slightly overcompensated as it lacks the single small overshoot seen in the simulated response. Based on the response in Figure 15 we estimate the implemented system has the characteristics listed in Table 11.

Characteristic	Measured System	Simulation
Phase Margin	55°	45°
Crossover Frequency	30 kHz	20 kHz

Table 11: *Estimated regulator characteristics based on the response to a 200 mA load step*

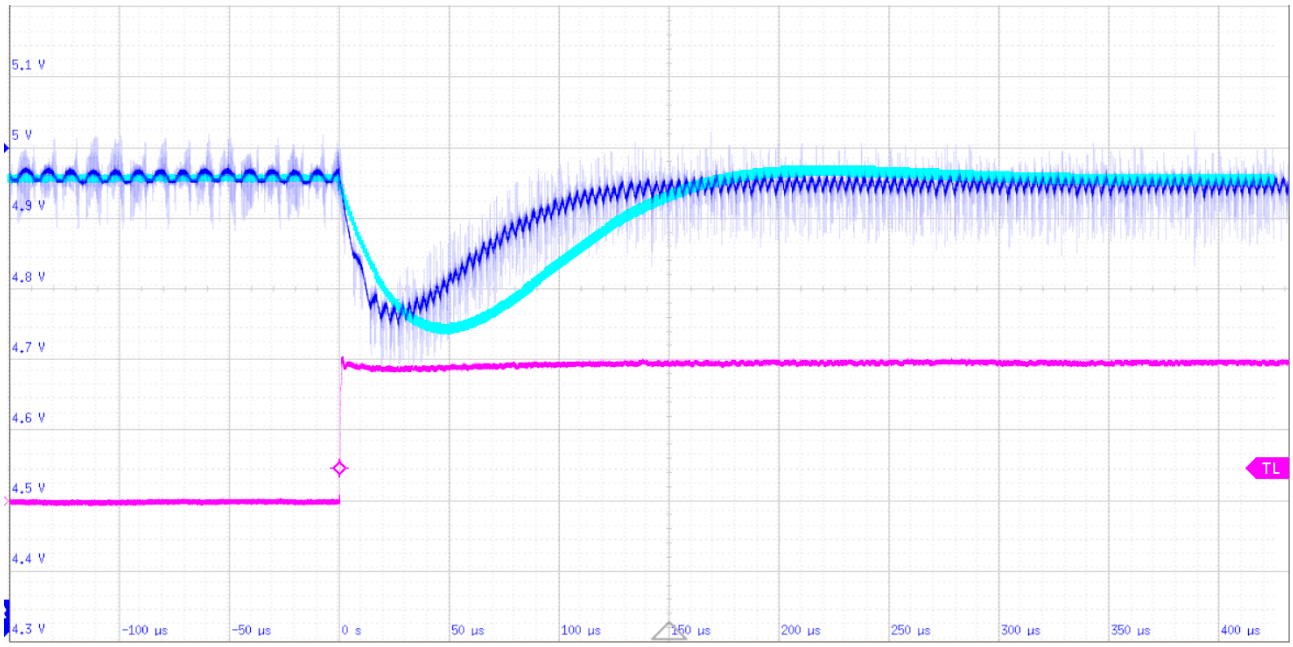

Figure 15: *Load regulation to a 200 mA load step for comparison between measured response and simulated response. Simulated response offset to remove constant load regulation error. Dark Blue: V_{OUT} measured; Light Blue: V_{OUT} simulated; Pink: I_{OUT} measured*

5.6.3 | Load Regulation

The output voltage with a 0 mA and 200 mA load can be seen in Figure 16 and Figure 17 respectively. The large ripple as well as the low frequency oscillating behavior are unintentional and are not present in the simulations conducted. The increased switching noise highlights the lack of switching during some periods of operation. Under correct operation, the switching should never cease and only the duty-cycle should change depending the load conditions and input to output voltage ratio. As can be seen by comparing both images, the period of the discontinuous switching cycles changes based on the load current,implying a connection to the regulators duty-cycle. It is suspected that an issue in current measurement circuit later described in subsection 6.2 could reasonable have influenced this behavior, although a clear causal link could not be established.

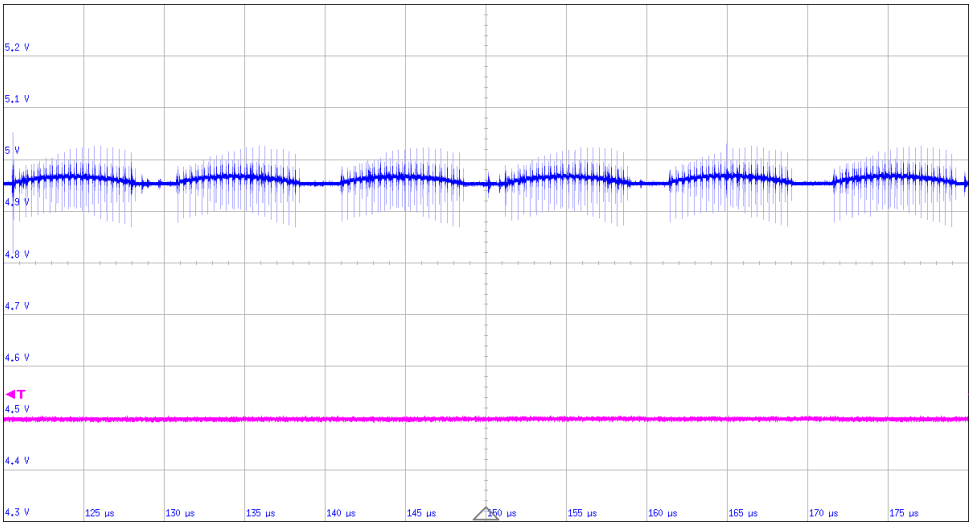

Figure 16: *Steady state load regulation with a 0mA load. Dark Blue: V_{OUT}; Pink: I_{OUT}*

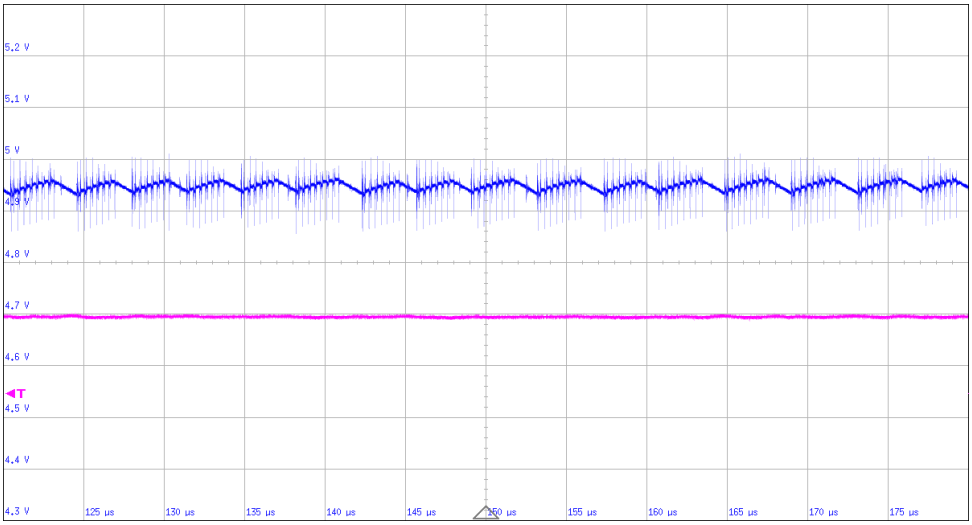

Figure 17: *Steady state load regulation with a 200mA load. Dark Blue: V_{OUT}; Pink: I_{OUT}*

5.6.4 | Efficiency

The conversion efficiency of our chip was measured under various load conditions and input voltage settings and can be seen in Figure 18. The measured results closely match our simulated values of 83.5 % at 200 mA load current regardless of the input voltage applied. The slight decrease in efficiency in comparison to the simulated values can be attributed to several not modeled effects such as bond wire resistance, losses in the input and output capacitors as well as losses else where outside of the IC. Of note is that the efficiency figures for 20 mA and 50 mA loads in Figure 18 were estimated by linearly interpolating the measured input power levels between 1 mA and 100 mA and then dividing the known output power level by the calculated input power estimate.

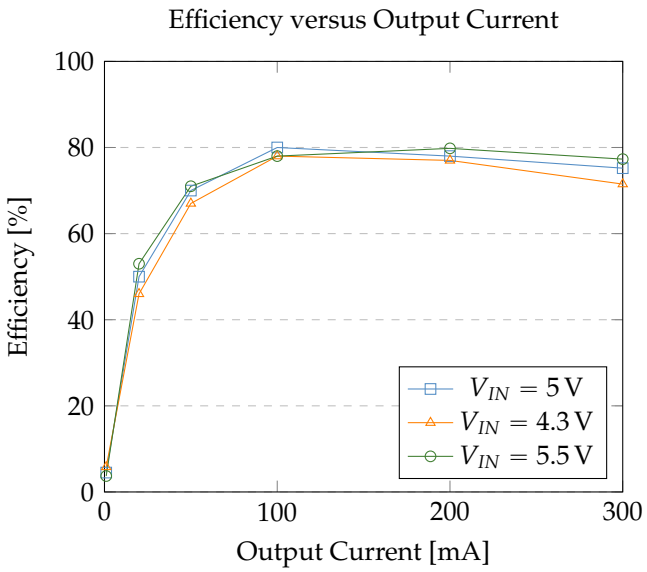

Figure 18: *Conversion efficiency at f_{SW} = 1.17 MHz; Data points for 20 mA and 50 mA are estimates based on interpolation*

5.6.5 | Conversion Losses

The total conversion losses can classified into two broad categories of switching frequency dependent switching losses P_{SWITCH} and load dependent conduction losses P_{COND} as shown in Equation 5.6.5. Our measured conversion losses can be seen in Figure 19 and shows a roughly 100 mW load independent loss, which explains the poor efficiency at sub 100 mA output currents. With increased output currents, the proportion of power loss due to switching decreases, leading to the improved efficiency in the 100 to 200 mA output current range. At large output current values >200 mA the conduction losses take over leading again to a decrease in efficiency.

$$P_{TOT} \approx P_{SWITCH} + P_{COND} \tag{1}$$

For an iso-frequency measurement as conducted in Figure 19, the switching losses appear as a constant offset as $P_{SWITCH} \propto 1$ and the conduction losses increase with the load current as $P_{COND} \propto I_{OUT}^2$. These contributions can be clearly seen in Figure 19 as a constant loss together with a quadratically increasing loss based on the load applied.

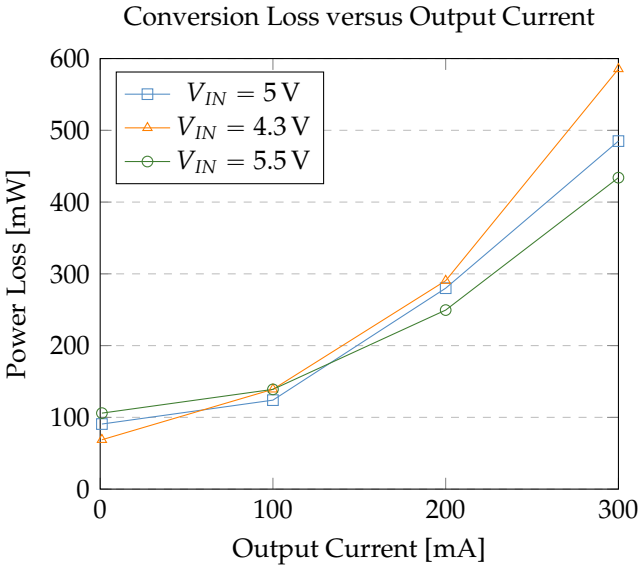

Figure 19: *Conversion losses at $f_{SW} = 1.17$ MHz*

5.7 Device Characteristics

The most critical device characteristics were compiled in to datasheet like table in Table 12 in order to give a high-level insight into the device operation and to compare the measured values with the results obtained from simulations.

Parameter	Information & Test Conditions	Sim	Min	Max	Unit
Buck-Boost Converter					
V_{OUT}	Average output voltage	5.01	4.99	5.03	V
$V_{OUT,PP}$	Ripple voltage on V_{OUT}, I_{LOAD} = 200 mA	13.2		200	mV
Line Regulation	V_{IN} = 4.3 - 5.5 V, I_{LOAD} = 200 mA	< 1		< 1	%
Load Regulation	V_{IN} = 5.0 V, I_{LOAD} = 0 - 200 mA	< 1		< 1	%
f_{SW}	Converter PWM frequency	1000	1170	2630	kHz
η	Efficiency @ f_{SW} = 1 MHz, I_{LOAD} = 200 mA	83.48		80.0	%
ω_0	Regulation loop crossover frequency	20		30	kHz
PM	Regulation loop phase margin	45		55	°
Current Consumption					
$I_{Q,VDDL}$	Quiescent current in V_{DDL}, V_{DDL} = 5 V, V_{RST} = 0 V	-		1.12	mA
$I_{IN,STBY}$	Input current V_{DDL} = V_{IN} = 5 V, I_{LOAD} = 0 mA	1.03		19	mA
$I_{SH,VDDL}$	Shutdown current in V_{DDL}, V_{DDL} = 5 V, V_{RST} = 5 V	-		< 10.0	µA
$I_{LEAK,VIN}$	Leakage current in V_{IN}, V_{IN} = 5 V, V_{RST} = 5 V	-		140	µA
Miscellaneous					
V_{UVLO}	Positive-going UVLO threshold voltage	3.4		3.72	V
$V_{FB} = V_{BGP}$	Internal FB reference voltage	1250	1239	1290	mV
I_{REF}	Internal reference current	10.5	14.11	14.88	µA
$R_{DS,on,HS}$	High-Side switch ON-Resistance	58.3			mΩ
$R_{DS,on,LS}$	Low-Side switch ON-Resistance	37			mΩ

Table 12: *Compilation of the main measured device characteristics compared with their simulated values*

6 Known Limitations

6.1 SPI Register Addressing Off-by-One Error

As illustrated in Table 5, register two is absent. This absence was not intentional but a consequence of historical developments. Initially, registers one and two were designed as read-only registers to provide status information about the chip, such as an over-temperature fault condition. However, it was later on decided not to implement these functionalities. Consequently, one register was eliminated, and a constant value was assigned to the remaining one (Register 1), as shown in Table 5. This modification was made a few weeks prior to the tape-out, and as a result to a tight timeline it was overlooked that the test bench and address mapping of the design must be updated to reflect this change. Therefore, to write to the first write register, the access must address register three instead of register two, as register two does not exist. While this is limitation does not impede functionality, it is an important consideration when accessing the registers.

6.2 Current Measurement Inaccurate if $V_{DDL} \neq V_{IN}$

The internal inductor current I_L measurement circuitry operates on the principle, that it amplifies the voltage drop over the input PMOS transistor. This approach works as the voltage drop during conduction can be approximated as

$$V_{DS,on} = R_{DS,on} \cdot I_L \tag{2}$$

leading to

$$I_L \approx \frac{V_{DS,on}}{R_{DS,on}} \tag{3}$$

As $R_{DS,on}$ is a known quantity and $V_{DS,on}$ can be directly measured, this approach can be used to measure the current flowing through the transistor. The on-resistance of the transistor is thus used as a current measurement shunt resistor. Equation 6.2 however only holds if the transistor is conducting current and thus the amplifier output is only valid in this case. In the non-conducting phase, the circuit would ordinarily still amplify the large voltage differential between source and drain leading to an output corresponding to a large inductor current. To combat this, we implemented a circuit to short the amplifier inputs when the input transistor is non-conducting, leading to an output corresponding to no inductor current. As the regulator implements peak-current mode control, the 0 current reading in the non-conducting phase leads to no problems and allows the circuit to start in the correct operating point when conduction starts.

In the implementation of the circuit we mistakenly shorted the inverting amplifier input V_M with the logic supply V_{DDL} instead of the converter power input V_{IN}, which is connected to the non-inverting amplifier input V_P as can be seen in Figure 20. In the simulation where $V_{DDL} = V_{IN}$ was always ued, this poses no problems as it does in practice when these conditions are applied. In cases where $V_{DDL} = V_{IN}$ is not applicable, the current measurement in the non-conducting phase generates an inaccurate current reading of large magnitude. This applies to cases where $V_{DDL} \neq V_{IN}$ is a static condition, e.g. $V_{DDL} = 5\,\text{V}; V_{IN} = 4.3\,\text{V}$, as well as for dynamic conditions such as when $V_{DDL} = V_{IN}$ set, but large current transient cause a voltage drop on V_{VIN}.

This issue could have various knock-on effects like the discontinuous regulation observed in subsubsection 5.6.3 but we could not prove this conclusively. The described issue could also exacerbate the issues with the start-up behavior as the large input current during start-up could lead to a voltage differential between V_{DDL} and V_{IN} causing issues in the current readings. A compounding issue is that any voltage transients get differently attenuated by the off-chip bypassing on both power-rails leading to unmeasurable dynamic errors in the current measurement.

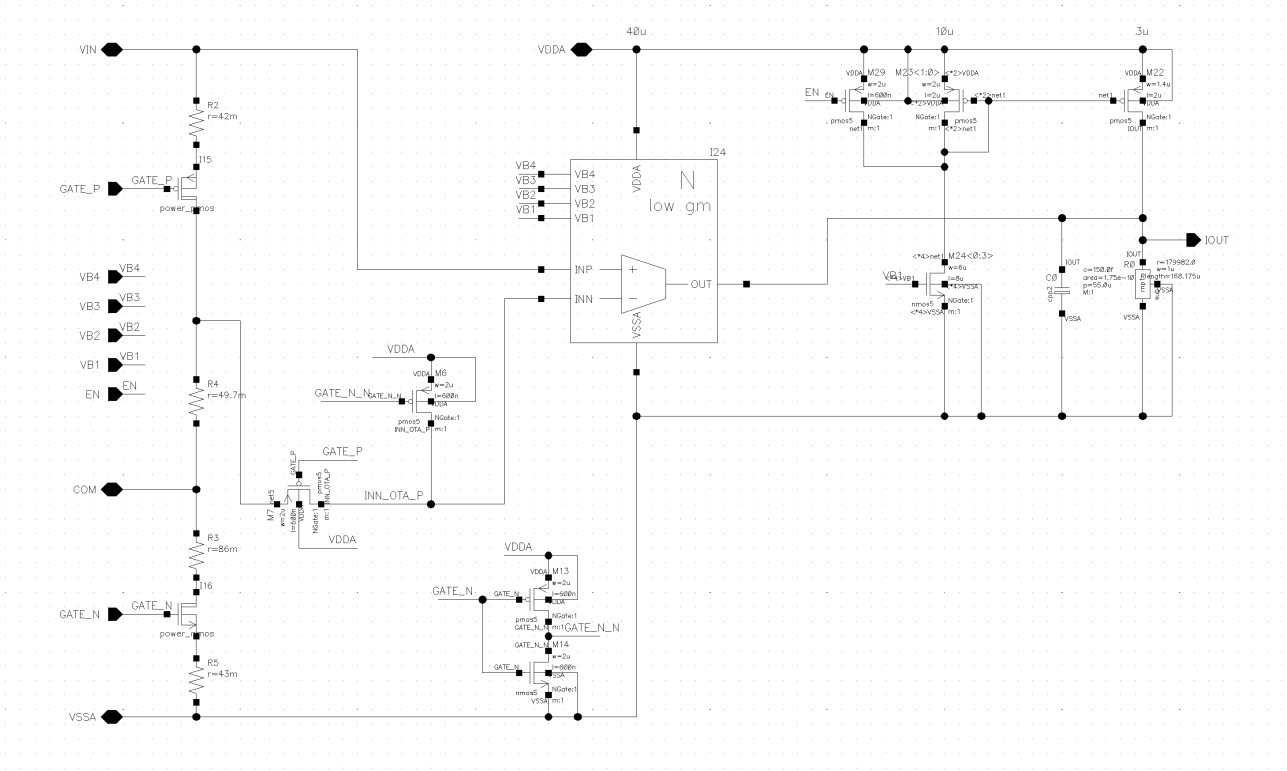

Figure 20: *Current measurement circuit with the error of connecting the source of M6 with VDDL (VDDA in this figure) instead of VIN*

6.3 Default Register Settings Disables Current Limit

A misconfiguration of the default state in the internal registers causes the current limit for the converter to be disabled at start-up. This causes the converter to start operating without an effective current limit leading to the converter pulling excessive amounts current at start-up, leading the supply to collapse to under the limit set by the POR. This behavior is documented in subsubsection 5.6.1. The current limit can be enabled after start-up and works as intended, but as the settings are stored in non-persistent memory, they are lost after restart and the chip therefore cannot begin operation with the current limit enabled.

6.4 Internal Current Reference Out of Specification

During testing, the internal current reference of the ASIC was discovered to be out of specification. The measured current was approximately 4 µA higher than the simulated value, representing a deviation of about 38.8%. While an exact cause for this discrepancy was not identified, it is hypothesized that the deviation may be attributable to the resistors used in the layout of the current reference.
The current reference plays a pivotal role in the ASIC, providing a stable reference current for various circuit components. Consequently, any deviation in the current reference can significantly affect the overall performance of the ASIC. Despite this, apart from some increased current consumption, the other blocks appeared to function as expected, even with the elevated current. However, the impact of the higher current is noticeable in certain blocks, such as the bandgap circuit. In the simulation, the voltage peaks over temperature is at 40 °C, but in the measurement with the higher current, it peaks at approximately 55 °C, as also discussed in subsection 5.3.
For more details on the current reference, please refer to subsection 5.4 and the corresponding figures.

6.5 Internal Oscillator Out of Specification

The internal oscillator of the ASIC was also found to be out of specification during testing. The measured frequency was significantly higher than the simulated value, resulting in a deviation of approximately 54.7% as it can be seen in subsection 5.5. Since this circuits frequency is not dependent on the current reference, but only on the bandgap voltage, the absolute value of an rnp1 resistor and MIM-capacitors, we find the resistor is the most likely issue.

7 | Conclusion

During this second phase of this project we successfully finished the chip design and were able to meet the tape-out deadline. The weeks leading up to this deadline were hectic and some of the mistakes described in section 6 could probably have been avoided with more time. In preparation to receiving the samples, we created the test setup described in section 4, creating both custom hardware and software for semi-automated chip testing from scratch. This allowed us to quickly start testing and gathering data as soon as the samples arrived. After some initial problems with the bring-up mainly caused by problems stemming from subsection 6.2, we are able to perform the automated tests we prepared and conduct more in depth manual testing of select samples. The automated tests lead to the device characterization described in subsection 5.7 and the manual measurements were used for diagnosing the issues described in section 6 and generate insights detailed in section 5.

We are overall very proud of what we were able to accomplish, given that the device mostly works as expected and this being the first chip we ever taped-out. While the mistakes in the current measurement circuit and in the default register configurations are disappointing, the high level functionality of the chip is preserved and we able to complete a large set of the tests we planed to conduct. Our test setup worked as designed with minimal need for fixes to the hardware or software after initial testing with the commercial chip.

The samples we characterized largely conform with the simulated values. We were however not able to find the reason behind the out of specification current reference and oscillator blocks. For both we lack adequate access to internal signals showing a lack of foresight with respect to DFT. This once again stems from the tight timeline leading up to the tape-out, leaving us with minimal time to carefully consider with signal to lead off-chip and to implement the required DFT structures for accurate probing. We were very pleased to see buck-boost converter working as intended, given our concerns with the current handling capabilities of the power stage and given the overall complexity of the regulator consisting exclusively custom designed IP blocks. As highlight, we were even able to characterize the chip with loads currents of 300 mA, an increase of 50 % over the designed maximum, while the chip maintained correct operation.

8 Outlook

As described, the designed ASIC achieves its main objectives and largely performs up to specification. It is therefore suitable as a basis for further design iterations or as a reference for incorporating some of the IP created into other designs. The identified limitations would need to be taken into consideration and changes would need to be implemented to remedy them. While the root cause for the current reference offset could not be found in the time attributed for troubleshooting, the issue does not appear to be insurmountable or a blocker for a redesign. The issues described with the digital circuitry could probably also be remedied with a limited amount of effort in a redesign. We therefore could forsee a continuation of this design.

The test setup could be further refined to allow for more in-depth testing as some manual testing steps carried could reasonably be automated. This would provide more detailed insights into the performance of the chip. For instance, the effects of the switching frequency on efficiency and power loss could be further investigated or the effects of temperature on the regulation characteristics could be recorded. In any case the test setup provides an extensible framework for ASIC validation and could be used for validation of other similar designs.

Finally, the project has demonstrated the potential of custom ASICs in the field of hearing instrument charging. With further development and refinement, these chips could play a crucial role in improving the efficiency and reliability of HI charging cradles. By incorporating the opportunities provided by high levels of integration the size of circuits can significantly be decreased while maintaining an extensive feature set.

9 | Declaration of Authorship

Declaration

We hereby declare that we have independently completed the present work without any assistance from third parties that were not mentioned in this document. We have only used the resources and tools that we have specified. Thoughts and ideas taken from external sources, whether directly or indirectly, have been appropriately acknowledged. The work has not been submitted to any other examination authority or previously published.

While composing this work, we utilized AI-assisted writing tools, specifically Copilot and ChatGPT for text optimization. Passages directly taken from the tool have been cited in the text as personal communication.

Place	**Date**
Rapperswil	July 11, 2024

Signature Matthias Meyer Patrick Jansky

10 | Listings

List of Abbreviations

ASIC Application Specific Integrated Circuit

DFT Design For Testing

DUT Device Under Test

HI Hearing Instruments

IC Integrated Circuit

LDO Low Drop-Out

NMOS N-Type Metal-Oxide Semiconductor

PCB Printed Circuit Board

PMOS P-type Metal-Oxide Semiconductor

POR Power-on-Reset

SPI Serial Peripheral Interface

USB Universal Serial Bus

List of Figures

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